LeCroy 9210
300 MHz Pulse Generator

Service Manual

LeCroy

Innovators in Instrumentation

9210-SM SOFTWARE
9210 UTILITIES
DISK 1 OF 1
VER 1.0
LeCroy
COPYRIGHT 1989 BY LECROY CORPORATION. LICENSED MATERIAL PROGRAM.
LECROY CORPORATION, 700 CHESTNUT RIDGE ROAD, CHESTNUT RIDGE, NY

OCT
92

LeCroy CORPORATION

Service Manual

9210/9211/9212/9213/9214
300 MHz Pulse Generator

October 1992

TABLE OF CONTENTS

Service Manual

9210 / 9211 / 9212 / 9213 / 9214 300 MHZ Pulse Generator

i.	Warranty	1
ii.	Product Assistance	2
iii.	Maintenance Agreements	2
iv.	Service Procedure	2

LECROY 9210 SERVICE MANUAL

1. GENERAL INFORMATION

1.0	Introduction	3
1.1	9210 Mainframe Specifications	4
1.1	9210 Mainframe Specifications (continued)	5

2. PERFORMANCE VERIFICATION

2.0	Introduction	6
2.1	Self Test	7
2.2	Period Accuracy Test	8
2.3	Delay Accuracy Test	9
2.4	Long Width Accuracy Test	11
2.5	Medium Width Test	12
2.6	Short Width Test	14
2.7	9210 Performance Verification Test Record	16
2.7.1	Self Test	16
2.7.2	Period Accuracy Test	16
2.7.3	Relative Delay Accuracy Test	17
2.7.4	Long Width Accuracy Test	18
2.7.5	Medium Width Test	19
2.7.6	Short Width Test	19

3. ADJUSTMENTS / CALIBRATION

3.0	Introduction	20
3.1	Equipment Requirements	20
3.2	External Triger Input Adjustment	20
3.3	Adjustment	21
3.4	CRT & Video Adjustments	22
3.4.1	Horizontal & Vertical Hold Adjustment	22
F 3.4	Video Display PC Board	22
3.4.2	Contrast and Brightness Adjustment	23
F 3.4.2	CRT with Display Background	23
3.4.3	Display Backround Adjustment	24
F 3.4.2.3	Effect of Contrast on Text	24
F 3.4.3.1	Centering Touch Screen Test on Display Background	25
F 3.4.3.2a	Location of CRT Alignment Tabs	25
F 3.4.3.2	Display Background Adjustment Examples	26

4. BASIC OPERATIONS/BLOCK DIAGRAMS

4.0	General Description	27
4.1	Power Supply	27
4.1.2	Video Sweep Board	28
4.1.3	Front Panel Board	28
4.1.4	Module Interconnections	29
4.1.5	Other Connections	29

9210 MAIN BASIC OPERATION

4.2	General Description	30
4.2.1	Microprocessor	31
4.2.2	Video Controller	32
4.2.3	Gpib Interface	32
4.2.4	Front Panel Interface	33
4.2.5	Measurement and Calibration System	33
4.2.6	Trigger Processing and Period Generation	34
4.2.7	Delay and Width Generation	35

BLOCK DIAGRAMS

F 4.1	9210 Block Diagram	36
F 4.1.1	Front Panel Board Block Diagram	37
F 4.1.2	Front Panel Scan Timing	38
F 4.1.3	Key Scan Table	39
F 4.2	9210 Main Block Diagram (1 of 2)	40
F 4.2	9210 Main Block Diagram (2 of 2)	41
F 4.2.1	uP Block Diagram	42
F .2.2	Block Diagram Video Section	43
F 4.2.3	Block Diagram Gpib	44
F 4.2.4	Block Diagram 9210 Front Panel Interface	45
F 4.2.5	Block Diagram 9210 Measurement System	46
F 4.2.6	Block Diagram Trig / Period	47
F 4.2.7	Block Diagram Delay / Width	48

5. DISASSEMBLY

5.0	Introduction	49
5.1	Power Supply	49
5.2	Power Supply Replacement	49
F 5.2.2	Bottom View	50
F 5.2.3	Rear View	50
F 5.2.6	Top View	51
F 5.2.5	Rear View	51
5.3	Fan	52
F 5.3.3	Rear View	52
5.4	Backplane Assembly	53
5.5	Mainboard	53
F 5.5.7	Mainboard Bottom Housing	54
F 5.5.8	9210 Mainboard to Backplane Cables	55
5.6	CRT and Video Assembly	56
F5.6.3	Side View	57
F 5.6.6	Front Panel Assembly	57
5.7	Front Panel PC Board and Soft Keys	58
F 5.7.3	Front Panel Knob Assembly	59
F 5.7.6	Front Panel Assembly (rear view)	59

6. 9210 MAINFRAME TROUBLESHOOTING

6.1	Introduction	60
6.2	9210 System	61
6.3	Calibration Failure	62
6.4	Self Test Failure	63
6.5	Power Supply	64
F 6.5.1	Power Supply Connector (P5) Pinout	65
6.6	Video Section	66
6.7	Front Panel	67
F 6.7.1	Touch CRT Control Signal Timing	68
F 6.7.2	Touch Key Example	68
F 6.7.3	Front Panel PC Board (solder side)	69
F 6.7.4	Touch CRT Key Detector signals	70
6.8	Processor Circuit	71
6.9	Trigger In	72
6.10	Trigger Out	73
6.11	Gpib	74
6.12	Backplane	75

7. SCHEMATICS

S1	9210 Main Schematics Rev B - 1	76
S2	9210 Main Schematics Rev B - 2	77
S3	9210 Main Schematics Rev B - 3	78
S4	9210 Main Schematics Rev B - 4	79
S5	9210 Main Schematics Rev B - 5	80
S6	9210 Main Schematics Rev B - 6	81
S7	9210 Main Schematics Rev B - 7	82
S8	9210 Main Schematics Rev B - 8	83
S9	9210 Main Schematics Rev B - 9	84
S10	9210 Main Schematics Rev B - 10	85
S11	9210 Main Schematics Rev B - 11	86
S12	9210 Main Schematics Rev B - 12	87
S13	9210 Main Schematics Rev B - 13	88

SCHEMATICS

F 7.1	9210 Assembly	89
F 7.2	9210 Front Panel Assembly	90
F 7.3	Front Panel Details A and B	91
S15	9210 Main Schematics Rev A - 1	92
S16	9210 Main Schematics Rev A - 2	93
S17	9210 Main Schematics Rev A - 3	94
S18	9210 Main Schematics Rev A - 4	95
S19	9210 Main Schematics Rev A - 5	96
S20	9210 Main Schematics Rev A - 6	97
S21	9210 Main Schematics Rev A - 7	98
S22	9210 Main Schematics Rev A - 8	99
S23	9210 Main Schematics Rev A - 9	100
S24	9210 Main Schematics Rev A - 10	101
S25	9210 Main Schematics Rev A - 11	102
S26	9210 Main Schematics Rev A - 12	103
S27	9210 Main Schematics Rev A - 13	104
S28	9210 Main Schematics Rev A - 14	105
S29	9210 Main Assembly Drawing	105a

8. PARTS LIST

8.0	1001: 9210 Parts List	106
8.1	1112: 9210 Main Parts List	107
8.1	1112: 9210 Main Parts List	108
8.1	1112: 9210 Main Parts List	109
8.1	1112: 9210 Main Parts List	110
8.1	1112: 9210 Main Parts List	111
8.1	1112: 9210 Main Parts List	112
8.1	1112: 9210 Main Parts List	113
8.1	1112: 9210 Main Parts List	114

MODULES SECTION

1. GENERAL INFORMATION

1.0	Introduction	115
1.1	9211 Module Specifications	116
1.2	9212 Module Specifications	117
1.3	9213 Module Specifications	118

2. PERFORMANCE VERIFICATION

2.0	Introduction	119
2.1	Self Test	120
2.2	Output Level DC Accuracy	120
2.3	Long Transition Time and Accuracy Test	121
2.4	Short Transition Time and Accuracy Test	122
2.5	9212 and 9214 Transition Time Range Test	123
2.6	Overshoot	124
2.7	9211 Performance Verification Test Record	126
2.7.1	Self Test	126
2.7.2	Output Level DC Accuracy	126
2.7.3	Long Transition Time Range Test (10% - 90%)	127
2.7.4	Short Transition Time Accuracy Test (10% - 90%)	127
2.7.6	Overshoot	128
2.8	9212 Performance Verification Test Record	129
2.8.1	Self Test	129
2.8.2	Output Level DC Accuracy	129
2.8.5	9212 Transition Time Range Accuracy Test (20% - 80%)	130
2.8.6	Overshoot	130
2.9	9213 Performance Verification Test Record	131
2.9.1	Self Test	131
2.9.2	Output Level DC Accuracy	131
2.9.3	Long Transition Time Accuracy Test (10% - 90%)	132
2.9.4	Short Transition Time Accuracy Test (10% - 90%)	133
2.9.6	Overshoot	133

PERFORMANCE VERIFICATION

2.10	9214 Performance Verification Test Record	134
2.10.1	Self Test	134
2.10.2	Output Level DC Accuracy	134
2.10.5	9214 Transition Time Range Test (20% - 80%)	135
2.10.6	Overshoot	135

3. ADJUSTMENTS / CALIBRATION

3.0	Introduction	136
3.1	Equiptment Requirements	136
3.2	LeCroy 9211 Adjustments	136
3.3	LeCroy 9212 Adjustments	136
3.5	LeCroy 9213 Adjustments	136
F 3.5.1	9213 AMP PC Board Adjustments	138
F 3.5.2	Composite Gain Adjustment	138
3.6	LeCroy 9214 Adjustments	139

4. BASIC OPERATION / BLOCK DIAGRAMS

4.0	General Description	140
4.1	9211 Basic Operation	141
4.1	General Description	141
4.1.1	HSC309	142
4.1.2	MSG305	142
4.1.3	HVV304	143
4.2	9212 Basic Operation	144
4.2	General Description	144
4.2.1	HLV308	144
4.2.2	9212 Functional Description	145
4.3	9213 Basic Operation	147
4.3	General Description	147
4.3.1	HSC309A	148
4.3.2	MSG305	149
4.4	9214 Basic Operation	150
4.4	General Description	150

4.4.1 HLV308 150

BLOCK DIAGRAMS

4.4.2 9214 Functional Discription 151
F 4.1 9211 Block Diagram 153
F 4.1.1 HSC309/HSC309A Block Diagram 154
F 4.1.2 MSG305 Block Diagram 155
F 4.1.3 HVV304 Block Diagram 156
F 4.2 9212 and 9214 Block Diagram (1 of 2) 157
F 4.2 9212 and 9214 Block Diagram (2 of 2) 158
F 4.2.1 HLV308 Block Diagram 159
F 4.2.2 9212 Pulse Shrinker 160
F 4.3 9213 Block Diagram 161

5. DISSASSEMBLY

5.0 Introduction 163
5.1 PC Board 163
5.2 PC Board Replacement 163
F M5.1.1 Module View (Left Side) 163
5.3 Module Front Panel PC Board 164
F M5.1.2 PC Board Removal 164
F M5.3.1 Module View (right side) 165
F M5.3.2 Module Front Panel (rear view) 165
5.4 9213 Output Module Amplifier Board 166
F M5.4.1 9213AMP and PC Board Removal 166

6. 92XX SERIES MODULE TROUBLESHOOTING

6.1 Introduction 167
M6.2 9211 Module 168
M6.2 9211 Module (Page 2) 169
M6.2 9211 Module (Page 3) 170
M6.2 9211 Module (Page 4) 171
6.2.1 9211 Module Troubleshooting 172
F 6.2.2A HVV304 Output Amplifier 173
F 6.2.2B HSC309 Slope Generator 174

MODULE TROUBLESHOOTING

M6.3	9212 and 9214 Module	175
M6.4	9213 Module	176
M6.4	9213 Module (Page 2)	177
M6.4	9213 Module (Page 3)	178
M6.4	9213 Module (Page 4)	179
6.5	9210 Communications Software (EVEDB)	180
6.5.1	Utility Programs Installation	180
6.5.2	Communication Software (EVEDB.EXE)	180
6.5.3	Disclaimer of Warranty and Implied Warranty	180
6.5.4	Requirements	180
6.5.5	Why We Distributed EVEDB.EXE	180
6.5.6	Overview of EVEDB Operation	181
6.5.7	Running EVEDB.EXE	182
6.5.8	General Rules	182
6.5.9	Using EVEDB	183
6.6	9211 Control File	184
6.7	Example of a Symbol Table (SYMBOL.MAP)	184

7. SCHEMATICS

S1	9211 PCB Schematics Rev A-1	185
S2	9211 PCB Schematics Rev A-2	186
S3	9211 PCB Schematics Rev A-3	187
S4	9211 PCB Schematics Rev A-4	188
S5	9211 PCB Schematics Rev A-5	189
	9211 PCB Diagram	190
S6	9212 PCB Schematics Rev C-1	191
S7	9212 PCB Schematics Rev C-2	192
S8	9212 PCB Schematics Rev C-3	193
S9	9212 PCB Schematics Rev C-4	194
S10	9212 PCB Schematics Rev C-5	195
S11	9212 PCB Schematics Rev C-6	196

SCHEMATICS

	9212 PCB Diagram	197
S12	9213 PCB Schematics Rev B-1	198
S13	9213 PCB Schematics Rev B-2	199
S14	9213 PCB Schematics Rev B-3	200
S15	9213 PCB Schematics Rev B-4	201
F 7.1	9211/9212/9213 Module Assembly	202
S16	9213 AMP Schematics Rev B-1 .	203
	9213 AMP Diagram	204
	9213 PCB Diagram	205
S17	9213 PCB Schematics Rev A-1	206
S18	9213 PCB Schematics Rev A-2	207
S19	9213 PCB Schematics Rev A-3	208
S19A	9213 PCB Schematics Rev A-3 (Prior to ECO 1005 Only)	209
S20	9213 PCB Schematics Rev A-4	210
S21	9213 AMP Schematics Rev A-1	211

8. PARTS LIST

8.0	1000: 9211 Parts List	212
8.1	1007: 9211 PCB Parts List	213
8.2	1000: 9212 Parts List	217
8.3	1206: 9212 PCB Parts List	218
8.4	1206: 9213 Parts List	223
8.5	1100: 9213 PCB Parts List	224
8.6	1000: 9214 Parts List	228

i. Warranty

LeCroy warrants the Models 9210, 9211, 9212, 9213 and 9214 to operate within specification under normal use and service for a period of 5 years from the date of shipment. Replacement parts, and repairs are warranted for "duration of the original warranty or one (1) year, whichever is longer". This warranty extends only to the original purchaser.

In exercising this warranty, LeCroy will repair or, at its option, replace any product returned to the Customer Service Department or an authorized service facility within the warranty period, provided that LeCroy's examination discloses that the product is defective due to workmanship or materials and has not been caused by misuse, neglect, accident or abnormal conditions or operations.

The purchaser is responsible for the transportation and insurance charges arising from the return of products to the servicing facility. LeCroy will return all in-warranty products with the transportation prepaid.

This warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. LeCroy shall not be liable for any special, incidental, or consequential damages, whether in contract, or otherwise.

ii. Product Assistance

Answers to questions concerning installation, calibration, and use of LeCroy equipment are available from the Factory headquarters, 700 Chestnut Ridge Road, Chestnut Ridge, New York USA 10977-6499. Call (914) 578-6020 and ask for SSD Customer Service or call your local field service office.

iii. Maintenance Agreement

LeCroy offers a selection of customer support services. Maintenance agreements provide extended warranty that allows the customer to budget maintenance costs after the intial warranty has expired. Other services such as installation, on-site repair, and addition of engineering improvements are available through Supplemental Support Agreements. Please contact the Customer Service Department or the local field service office for details.

iv. Service Procedure

Products requiring maintenance should be returned to an authorized service facility. If under warranty, LeCroy will repair or replace the product at no charge. The purchaser is only responsible for the transportation charges arising from return of the goods to the service facility.

For all LeCroy products in need of repair after the warranty period, the customer must provide a Purchase Order Number before any inoperative equipment can be repaired or replaced. The customer will be billed for the parts and labor for the repair as well as for shipping.

All products returned for repair should be identified by their model and serial numbers and include a description of the defect or failure, name and phone number of the user. In the case of products returned, a Return Authorization Number (RA#) is required and may be obtained by contacting the LeCroy Customer Service Department in your area or contact LeCroy (New York, USA) at (914) 425-6020.

LECROY 9210 SERVICE MANUAL

General Information

1.0 Introduction

This service manual contains information to maintain the LeCroy 9210 Pulse Generator Mainframe and Output Modules. The manual is divided into eight sections as follows:

1. General Information
   Contains the Model 9210 description, specifications, and characteristics.

2. Performance Verification
   Contains the performance tests necessary to verify instrument specifications, including recommended test equipment and test record form.

3. Adjustments / Calibration
   Contains the necessary procedures to adjust the instrument after servicing.

4. Basic Operation / Block Diagrams
   Contains operation descriptions and block diagrams for the instrument.

5. Disassembly
   Contains the disassembly and assembly procedures.

6. Toubleshooting
   Contains troubleshooting flowcharts to assist in the repair of the instrument.

7. Schematics / Reference Drawings
   Contains schematic and component location diagrams.

8. Parts List
   Contains the instument's parts list.

Refer to the LeCroy Model 9210 Operator's Manual for information on operating and programming.

This manual provides replaceable subassembly service information and is not intended to support component level troubleshooting.

1.1 LeCroy 9210
300 MHz Programmable Pulse Generator Mainframe Specifications

Important Note: *At least one Output Module (9211, 9212, or 9213) must be installed in the 9210 Pulse Generator Mainframe in order to obtain a pulse output.*

Timing Characteristics:

Defined at 50% amplitude points and minimum transition times.

NOTE: The minimum values listed below refer to the mainframe only, and may not be achievable with all output modules.

Pulse Period: 3.33 nsec to 450 msec.

Resolution: the greater of 0.1% of value or 10 psec
Accuracy: ± (0.5% of value + 0.2 nsec) from 3.33 nsec to 450 msec
RMS Jitter: ≤0.035% (350 ppm) of value + 35 psec
Temperature Coefficient: <250 ppm/°C typ. with Temperature Compensation ON

Frequency: Alternate format for Period. Settable from 300 MHz to 2.2 Hz with 0.1% resolution.

Pulse Width: 1.0 nsec to 450 msec
For Period setting ≤ 8.0 nsec:
Max. Width = Period - 0.8 nsec
For Period setting > 8.0 nsec:
Max. Width = Period - 2.9 nsec

Resolution: the greater of 0.1% of value or 10 psec
Accuracy: ± (0.5% of value + 0.3 nsec + transition time error) from 1.6 nsec to 450 msec (see Output Module data for transition time accuracy specifications)
RMS Jitter: ≤0.035% of value + 35 psec
Temperature Coefficient: <250 ppm/°C typ. with Temperature Compensation ON

Duty Cycle: Alternate format for Width. Settable from 1% to 99% in 0.01% steps. In this format, Width is controlled as a percentage of Period

Pulse Delay: 0 nsec to 450 msec, measured from leading edge of Trigger Out to beginning of leading edge of Pulse Output (relative to fixed offset).
For Period setting ≤ 8.0 nsec:
Max. Delay = Period - 2.6 nsec
For Period setting > 8.0 nsec:
Max. Delay = Period - 4.7 nsec

Resolution: the greater of 0.1% of value or 10 psec
Accuracy: ±(0.5% of value + 1.0 nsec)
RMS Jitter: ≤0.035% of value + 35 psec
Temperature Coefficient: <(250 ppm +50 psec)/°C typ. with Temperature Compensation ON
Match Between Output Modules of the same type: 1.2 nsec

Phase: Alternate format for delay. Settable from 0° to 359.9° with 0.1° resolution. In this format, Delay = Phase/360 x Period.

Double Pulse Delay: 4 nsec to 450 msec
Resolution: the greater of 0.1% of value or 10 psec
Accuracy: ± (0.5% of value + 0.3 nsec)
RMS Jitter: ≤0.035% of value + 35 psec
Temperature Coefficient: <250 ppm/°C typ. with Temperature Compensation ON

Inputs and Outputs:

External Input:

Input Impedance: 10 kΩ or 50 Ω ± 5%, selectable
Input Range: ±5 V into 50 Ω or ± 20 V into 10 kΩ
Minimum Detectable Amplitude: 200 mV
Threshold range and resolution: ±2.5 V adjustable in 20 mV steps
Threshold Level Accuracy ±100 mV
Max. Input Frequency: 300 MHz
Min. Pulse Width: 1.5 nsec
Min. Input Slew Rate: 10 V/sec
Edge Selection: Positive, Negative, neither edge (disabled).

Trigger Output:

Output Levels: Nominal 1 V negative swing from base level into 50 Ω. Base level adjustable over ±1.5 V range with 20 mV resolution. (Into Hi-Z: Amplitude = –2 V. Base level of ±3 V, 40 mV resolution)
Output Impedance: 50 Ω ±5%
Protection: Protected against application of ±10 V.
Delay from Trigger Input: 21 nsec typ.

Width: Dependent on Trigger Mode:

Normal Mode:
Period ≤ 7.2 nsec:
Width = 1.8 nsec typ.
7.2 nsec < Period < 50 nsec:
3.6 nsec ≤ Width ≤ 7.2 nsec
Period ≥ 50 nsec:
Width = 25 nsec typ.

Single Mode:
Pulse Width setting ≤ 40 nsec:
Trigger Output Width = 1.8 nsec typ
Pulse Width setting > 40 nsec:
Trigger Output Width = 25 nsec typ.

Burst Mode:
Width=Period x (Burst Count - 1)

Gate and Ext. Width Modes:
Trigger Output Width ≈ Trigger Input Width

300 MHz Programmable Pulse Generator Mainframe Specifications (continued)

Programmability:

All generator functions are programmable over GPIB. Command set conforms with IEEE 488.2-1987.

Triggering Modes:

Normal: Continuous pulse stream. One trigger output for each pulse output.

Single: Each external trigger input generates a single output pulse. One trigger output for each trigger.

Gated: Signal at external input enables period generator. The first output pulse is synchronized with the gate's leading edge. Last pulse is allowed to complete. One trigger output for each Gate input. 20 nsec retrigger (dead) time between Gate inputs.

Burst: Each external trigger input generates a pre-programmed number of pulses (3 to 4095). Minimum time between two bursts is 50 nsec. One trigger output for each trigger.

External Width: The signal at the external input is reproduced with programmable transition times and output levels. One Trigger Output for each external trigger input.

Operating Features:

Manual Trigger: Front panel pushbutton generates an external trigger input. Each push provides one trigger pulse in Single and Burst Modes. Output remains active as long as button is pressed in Gate and External Width Modes.

Double Pulse Mode: When double pulse is set to ON, two pulses are produced for each trigger. The first pulse begins as soon as possible after the trigger (approximately the minimum Pulse Delay time). The Delay parameter now specifies the time from the leading edge of the first pulse to the leading edge of the second pulse. One trigger output occurs for each pulse pair. Compatible with all trigger modes except External Width.

Additional Capabilities:

Limit: When enabled, the maximum high and low level settability of the pulse outputs is limited to protect the device under test.

Setups: 16 setup configurations can be stored and recalled using the Store and Recall keys on the front panel.

Change Format: Enables the alternate representation of a parameter or enables an alternate mode of operation. Examples are Amplitude/Base or Amplitude/Median in lieu of VHigh/Vlow, Duty Cycle instead of Width, Phase instead of Delay, Frequency instead of Period, Slew Rate as opposed to Transition Time.

Environmental:

The following specifications apply to the 9210 mainframe and to all output modules (9211, 9212 and 9213)

Storage Temperature: -40°C to 70°C (temp above 40°C may degrade battery life)

Operating Temperature: 5°C to 40°C at rated specifications, operational from 0°C to 50°C

Temperature & Self-Calibration: Generator and Output Modules will meet specifications over a ± 5°C range without repeating Self-Calibration

Humidity Range: < 95% R.H from 5°C to 40°C

Power:

115/220 VAC ± 20%; 48 - 448 Hz. 300 Watts Max. (180 typ)

Miscellaneous:

Battery Backup Life: 10 years typ.

The following specifications apply to the 9210 mainframe and to all output modules (9211, 9212 and 9213)

Recalibration Interval: 1 year

Warmup Time (to meet specs): 15 min, after which a new Self-Calibration must be performed

9210 Mainframe:

Weight:	23 lbs. net 34 lbs. shipping.
Dimensions:	Height: 5" Width: 17" Depth: 21"

Output Modules:

Weight:	2 lbs. net 4 lbs. shipping
Dimensions:	Height: 4.6" Width: 2.4" Depth: 14.7"

Options:

9210/SM Service Manual
9210/RM Rack Mount Kit

LECROY 9210 PULSE GENERATOR
Mainframe Performance Verification Procedure

2.0 Introduction

This procedure can be used to verify the main operating specifications of the LeCroy 9210 pulse generator mainframe. It is useful as a calibration verification procedure as well as an incoming inspection checkout.

Equipment Required

The procedure was designed so that the measurements are able to be done with the widest range of instruments. For this reason, we have sometimes chose a less efficient means of making a measurement in order to accomodate a wider range of instruments. In this way we hope to be able to support as many customers requirements as possible.

Description	Performance Requirements	Recommended Models
Time interval counter (TIC)	300 MHz frequency A to B, period, width, rise, fall interval accuracy <2.5ns	**Stanford Research Systems 620** HP 5335A HP 5334B A digital oscilloscope with adequate accuracy may be used.
Sampling Scope	5 GHz bandwidth	**TEK 7603 with 7T11/7S11 & S-2** HP 54120 series TEK 11800 series
Synthesizer (signal generator)	Frequency > 300MHz Freq. acc. < 1000 ppm	**Marconi 2022** HP 8656B
LeCroy 9212 or 9214 Output module		**LeCroy 9212 or 9214 Output module**

Preliminary setup

1. Install output module in Channel A slot (Install 2nd output module in channel B if available).
2. Power up 9210 and allow at least 15 minute warmup period.
3. Retrieve default setup in the pulse generator. Do this on the pulse generator by recalling the standard settings. The following default settings will be applied:

setting	value	change	setting	value	change
CHANNEL:			TRIGGER:		
Amplitude	500 mV		Mode	Normal	
Median	0 V		Burst count	3	
Duty cycle	20%		Level	0.1 V	
Delay	0 ns		Slope	+	
Lead	0.4 ns				
Trail	0.4 ns		MODULE:		
Period	100 ns		Invert	off	
			Disable	on	

2.1 Self Test

1. Bring up the "MORE" menu on 9210 and press "CAL" to intiate self-calibration.
2. Check that unit passed self calibration. Enter result on Test Report.
3. Bring up the "MORE" menu on 9210 and press "SELF TEST" to initiate self test.
4. Check that unit passed self test. Enter result on Test Report.

2.2 Period Accuracy Test

Specification

± (0.5% of setting + .2 nsec)

Summary

Period accuracy is checked over full range of pulse generator utilizing the time interval counter.

Equipment

1. Time interval counter
2. LeCroy 9212 or 9214 Pulse generator module

Setup

1. Adjust settings of pulse generator as shown in table below. Note that only settings with an x in the change column need to be changed if you are following the order of the procedure.

setting	value	change	setting	value	change
CHANNEL:			TRIGGER:		
Amplitude	5.0 V	x	Mode	Normal	
Median	0 V		Burst count	3	
Duty cycle	50%	x	Level	1 V	x
Delay	0 ns		Slope	+	
Lead	0.3 ns	x			
Trail	0.3 ns		MODULE:		
Period	100 ns		Invert	off	
			Disable	off	x

2. Cable output of module to Channel A input of time interval counter.
3. Set following settings on time interval counter:

Setting	Value
Mode	period
Trigger level	0 V
Gate duration	0.01 sec

4. Time interval counter should be reading 100 nsec period.

Procedure

1. Set 9210 to the period shown in line 2.1 of the Test Record and measure period on time interval counter.
2. Record measurement from time interval counter in line 2.1 of the Test Record.
2. Repeat steps 1 and 2 for lines 2.2 to 2.10 of the Test Record.

2.3 Delay Accuracy Test

Specification

± (0.5% of setting + 1.0 nsec)

Summary

The delay accuracy of the 9210 is tested in decade ranges over the full range of operation utilizing the time interval counter. The procedure assumes that the time interval counter has a "relative mode" to eliminate the need to subtract the fixed delay from all the measurements. If the time interval counter you are using does not have a "relative mode" then it is necessary to subtract the fixed delay from all the measurements before comparing to the given limits.

Equipment

1. Time interval counter
2. LeCroy 9212 or 9214 output module

Setup

1. Set pulse generator settings as shown in table below.

setting	value	change	setting	value	change
CHANNEL:			TRIGGER:		
Amplitude	5.0 V		Mode	Normal	
Median	0 V		Burst count	3	
Duty cycle	50%		Level	1 V	
Delay	0 ns		Slope	+	
Lead	0.3ns				
Trail	0.3ns		MODULE:		
Period	250 ms	x	Invert	off	
			Disable	off	

2. Set time interval counter as indicated below:

Setting	Value
Mode	Time interval , A to B
A Trigger level	-0.5 V
A Trigger slope	-
A coupling	DC, 50 Ω term
B Trigger level	0 V
B Trigger slope	+
B Coupling	DC, 50 Ω term

3. Make sure Time interval counter "relative mode" is cleared.
4. Time interval counter should read about 10 nsecs ± 4 nsecs
5. SET "relative mode" on time interval counter so that all delay measurements are made relative to this fixed offset.

Procedure

1. Set 9210 to the delay shown in line 3.1a of the Test Record.
2. Record measurement in line 3.1a of the Test Record.
3. Repeat steps 1 and 2 for lines 3.2a to 3.10a of the Test Record
4. Clear "relative mode" of time interval counter.

2.4 Long Width Accuracy Test

Specification

± (0.5% of setting + 0.3 nsec)

Summary

Accuracy of the longer pulse width range is checked with the time interval counter.

Equipment

1. Time interval counter
2. LeCroy 9212 or 9214 output module

Setup

1. Set pulse generator settings as shown in table below.

setting	value	change	setting	value	change
CHANNEL:			TRIGGER:		
Amplitude	5.0 V	.	Mode	Normal	
Median	0 V		Burst count	3	
Width	2 us	x	Level	1 V	
Delay	0 ns		Slope	+	
Lead	0.3 ns				
Trail	0.3 ns		MODULE:		
Period	300 ms	x	Invert	off	
			Disable	off	

2. Set time interval counter as indicated below:

Setting	Value
Mode	Width
Trigger level	0 V
Trigger slope	+
Coupling	DC, 50 Ω term

3. Cable the output of the module to the time interval counter.
4. Time interval counter should be reading 2 usec.

Procedure

1. Record the measured width from the Time interval counter on line 4.1a of the Test Record.
2. Set the pulse generator width to the value in the next line of the Test Record.
3. Record the measured width on that line.
4. Repeat steps 2 and 3 for lines 4.2 through 4.10.

2.5 Medium Width Test

Specification

± (0.5% of setting + 0.3 nsec)

Summary

This setup is used to measure pulse widths between 10 nsec and 500 nsec. To allow use of the broadest range of sampling scopes (both analog and the newer digital types) this procedure does not make stringent demands on the time accuracy of the scope. Instead, the scope is used to measure the difference between a sine wave period generated by a synthesizer and the width of the pulse output by the 9210. In this way the measurement setup can achieve the required 0.125% accuracy needed to verify the width accuracy of the 9210. The medium width measurement can be measured directly by using a HP54100 series or equivalent oscilloscope. The deviation is the difference between the 9210 width setting and the oscilloscope measurement of the width.

Equipment

1. Sampling oscilloscope
2. Synthesizer
3. LeCroy Model 9212 or 9214 output module
4. BNC Tee

Setup

1. Set pulse generator settings as shown in table below.

setting	value	change	setting	value	change
CHANNEL:			TRIGGER:		
Amplitude	1.0 V	x	Mode	Single	x
Median	0 V		Burst count	3	
Width	10 ns	x	Level	0 V	x
Delay	25 ns	x	Slope	+	
Lead	0.3 ns		Impedance	HI Z	x
Trail	0.3 ns		MODULE:		
Period	1.5 us	x	Invert	off	
			Disable	off	

2. Cable output of module to channel 1 input of the sampling scope.
3. Connect a BNC Tee onto the trigger input of the 9210.
4. Cable output of synthesizer to one side of the BNC Tee at the 9210 trigger input.
5. Cable other side of BNC Tee to channel 2 input of sampling scope.
6. Set the synthesizer to 0 dbm amplitude, and 100 MHz frequency.
7. Set sampling scope to trigger on channel 1 (pulse generator output) and adjust scope delay control to view both pulse and synthesizer output simultaneously.

Procedure

1. Adjust scope offset of channel 1 so that the pulse 50% amplitude level is centered on the vertical grid centerline.
2. Adjust the scope offset of channel 2 so that the sine wave is centered around the vertical grid centerline. Also adjust scope gain so that the sine wave is shown as large as possible on the screen.
3. Adjust pulse generator delay to roughly align a zero crossing of the sine wave with the leading edge of the output pulse.
4. Now expand the timebase of the scope around the leading edge of the pulse to the time/division shown on the test report for the current step.
5. Adjust delay finely to align zero crossing of sine wave with leading edge of pulse to within 1 minor division.
6. Now adjust scope timebase delay to view falling edge of pulse. Do not change time/division.
7. Now read time difference between falling edge of pulse and closest zero crossing of sine wave to within 1 minor division. Record reading in test record.
8. Set synthesizer to frequency shown in next step.
9. Set pulse generator to width and delay shown in next step.
10. Set sampling scope to time/division shown in next step.
11. Repeat steps 3 to 11 for rest of test record entries.

2.6 Short Width Test

Specification

± (0.5% of setting + 0.3 nsec)

Summary

This setup is used to measure pulse widths between 1.6 nsec and 5 nsec. For this range the width can be measured directly on the sampling scope.

Equipment

1. Sampling oscilloscope
2. LeCroy Model 9212 or 9214 output module

Setup:

1. Set pulse generator settings as shown in table below.

setting	value	change	setting	value	change
CHANNEL:			TRIGGER:		
Amplitude	1.0 V		Mode	Normal	x
Median	0 V		Burst count	3	
Width	5 ns	x	Level	0 V	
Delay	0 ns	x	Slope	+	
Lead	0.3 ns		Impedance	HI Z	
Trail	0.3 ns		MODULE:		
Period	1.5 us	x	Invert	off	
			Disable	off	

2. Cable output of module to channel 1 input of the sampling scope.
3. Set sampling scope to trigger on channel 1 (pulse generator output) and adjust to view pulse.

Procedure

1. Adjust scope offset of channel 1 so that the pulse 50% amplitude level is centered on the vertical grid centerline.
2. Set sampling scope to time/division shown in step and measure width to within 1 minor division.
3. Record measurement in test record.
4. Set pulse generator to width shown in next step.
5. Repeat steps 2 to 3 for rest of test record entries.

2.7 9210 PERFORMANCE VERIFICATION TEST RECORD

TESTED BY: _____ PASSED:____ FAILED:____

SERIAL NUMBER: _____ DATE: _____

COMMENTS:

_____

_____

_____

_____

2.7.1 Self Test

1.1 Self Calibration Pass____ Fail____

1.2 Self Test Pass____ Fail____

_____

2.7.2 Period Accuracy Test

Step	Set Period	Lower Limit	Measured Period	Upper Limit	Pass	Fail
2.1	3.33 ns	3.112 ns	_____	3.547 ns	____	____
2.2	10.00 ns	9.750 ns	_____	0.25 ns	____	____
2.3	100.0 ns	99.30 ns	_____	100.70 ns	____	____
2.4	1.00 us	.9948 us	_____	1.005 us	____	____
2.5	10.00 us	9.95 us	_____	10.05 us	____	____
2.6	100.0 us	99.5 us	_____	100.5 us	____	____
2.7	1.00 ms	.995 ms	_____	1.005 m	____	____
2.8	10.00 ms	9.95 ms	_____	0.05 ms	____	____
2.9	100.0 ms	99.5 ms	_____	100.5 ms	____	____
2.10	500.00 ms	497.5 ms	_____	502.5 ms	____	____

2.7.3 Relative Delay Accuracy Test

Period set to 250 msec. Measured delay with fixed offset removed.

CHANNEL A

Step	Set Delay	Lower Limit	Measured Delay	Upper Limit	Pass	Fail
3.1a	2 ns	1.00 ns	_____	2.00 ns	____	____
3.2a	5 ns	3.97 ns	_____	6.03 ns	____	____
3.3a	10 ns	8.95 ns	_____	11.05 ns	____	____
3.4a	100 ns	98.5 ns	_____	101.5 ns	____	____
3.5a	1 us	0.994 ns	_____	1.006 us	____	____
3.6a	10 us	9.949 us	_____	10.051 us	____	____
3.7a	100 us	99.50 us	_____	100.5 us	____	____
3.8a	1 ms	0.995 us	_____	1.005 ms	____	____
3.9a	10 ms	9.95 ms	_____	10.05 ms	____	____
3.10a	100 ms	99.5 ms	_____	100.5 ms	____	____

CHANNEL B

Step	Set Delay	Lower Limit	Measured Delay	Upper Limit	Pass	Fail
3.1b	2 ns	1.00 ns	_____	2.00 ns	____	____
3.2b	5 ns	3.97 ns	_____	6.03 ns	____	____
3.3b	10 ns	8.95 ns	_____	11.05 ns	____	____
3.4b	100 ns	98.5 ns	_____	11.05 ns	____	____
3.5b	1 us	0.994 us	_____	1.006 us	____	____
3.6b	10 us	9.949 us	_____	10.051 us	____	____
3.7b	100 us	99.50 us	_____	100.5 us	____	____
3.8b	1 ms	0.995 ms	_____	1.005 ms	____	____
3.9b	10 ms	9.95 ms	_____	10.05 ms	____	____
3.10b	100 ms	99.5 ms	_____	100.5 ms	____	____

2.7.4 Long Width Accuracy Test

Period set to 300 msec.

CHANNEL A

Step	Set Width	Lower Limit	Measured Period	Upper Limit	Pass	Fail
4.1a	2 us	1.990 us	_____	2.010 us	____	____
4.2a	10 us	9.95 us	_____	10.05 us	____	____
4.3a	100 us	99.5 us	_____	100.5 us	____	____
4.4a	1 ms	0.995 ms	_____	1.005 ms	____	____
4.5a	10 ms	9.95 ms	_____	10.05 ms	____	____
4.6a	100 ms	99.5 ms	_____	100.5 ms	____	____
4.7a	250 ms	248.8 ms	_____	251.25 ms	____	____

CHANNEL B

Step	Set Width	Lower Limit	Measured Period	Upper Limit	Pass	Fail
4.1b	2 us	1.990 us	_____	2.010 us	____	____
4.2b	10 us	9.95 us	_____	10.05 us	____	____
4.3b	100 us	99.5 us	_____	100.5 us	____	____
4.4b	1 ms	0.995 ms	_____	1.005 ms	____	____
4.5b	10 ms	9.95 ms	_____	10.05 ms	____	____
4.6b	100 ms	99.5 ms	_____	100.5 ms	____	____
4.7b	250 ms	248.8 ms	_____	251.25 ms	____	____

2.7.5 Medium Width Test

CHANNEL A

Step	Set Width	Rough Delay	Synth Freq	Lower Limit	Measured Period	Upper Limit	Pass	Fail
5.1a	10 ns	25 ns	100 MHz	-0.38 ns	_____	0.38 ns	____	____
5 2a	100 ns	250 ns	10 MHz	-0.8 ns	_____	0.8 ns	____	____
5 3a	500 ns	1.1 us	2 MHz	-2.8 ns	_____	2.8 ns	____	____

CHANNEL B

Step	Set Width	Rough Delay	Synth Freq	Lower Limit	Measured Period	Upper Limit	Pass	Fail
5.1b	10 ns	25 ns	100 MHz	-0.38 ns	_____	0.38 ns	____	____
5 2b	100 ns	250 ns	10 MHz	-0.8 ns	_____	0.8 ns	____	____
5 3b	500 ns	1.1 us	2 MHz	-2.8 ns	_____	2.8 ns	____	____

2.7.6 Short Width Test

CHANNEL A

Step	Set Width	Lower Limit	Measured Period	Upper Limit	Pass	Fail
6.1a	5.0 ns	4.675 ns	_____	5.325 ns	____	____
6.2a	1.6 ns	1.29 ns	_____	1.91 ns	____	____

CHANNEL B

Step	Set Width	Lower Limit	Measured Period	Upper Limit	Pass	Fail
6.1b	5.0 ns	4.675 ns	_____	5.325 ns	____	____
6.2b	1.6 ns	1.29 ns	_____	1.91 ns	____	____

ADJUSTMENTS

3.0 Introduction

This section includes the adjustments required for the instrument. It is recommended that they be verified at one year intervals.

NOTE ***If it is not possible to make any of the following adjustments, refer to the t troubleshooting section of this manual.***

3.1 Equipment Requirements

INSTRUMENT	SPECIFICATION
Synthesize or Pulse Generator with a 1% or better amplitude accuracy	100 KHz, Square Wave 1 V pk-pk
Oscilloscope	> 5 MHz bandwidth

3.2 External Trigger Input Adjustment

SETUP

1. Connect a 100 KHz, 1 V p-p (-0.5 V to +0.5 V), Square Wave to the 9210 External Input.

2. Insert a LeCroy 9211, 9212, 9213, or 9214 Output Module into the 9210 and power on the instrument. Allow a 5 minute warm-up period prior to adjustments.

3. Connect the Output module to the Oscilloscope. Set the O'scope as follows: 1 us per div., 0.5 V per div., 50 Ohm input termination

4. Recall STANDARD SETUP.
   Press the **RECALL SETUP** key (Changes display to Setup Menu).
   Press the **ENTER** key twice.

5. Set WIDTH to 1 us.
   Press the **1** key and **u/Mhz** key.

   NOTE ***Conflict warnings (???) will be displayed at this point.***

6. Set Trigger to for SINGLE TRIGGER MODE.
   Press the **TRIGGER** key (Changes display to trigger menu).
   Press the **ENTER** key (Changes mode from Normal to Single).

7. Enable the Output Module.
   Press **DISABLE** key on Output Model.

8. Setup the Trigger Level.
   Select **LEVEL** on Trigger menu (may use Touch keys or Select keys).

3.3 Adjustment

1. Rotate the FINE CONTROL KNOB clockwise, increasing the Trigger Level. Note the level at which the waveform disappears. Reset the Trigger Level to 0.10 V.

2. Rotate the FINE CONTROL KNOB counter-clockwise, decreasing the Trigger Level. Note the level at which the waveform disappears. Reset the Trigger Level to 0.10 V.

3. Add the results of Steps 1 and 2. Divide the value by two and subtract the result from the value in Step 1. Rotate the FINE CONTROL KNOB to adjust the Trigger Level to this new value.

4. Adjust R66 to the point that the waveform just disappears.

5. Using the FINE CONTROL KNOB adjust the Trigger Level to 0.52v.

6. Adjust C11 to the point that the waveform just disappears.

7. Using the FINE CONTROL KNOB verify:

TRIGGER LEVEL	WAVEFORM
0.50	stable pulse
0.52	no pulse
-0.50	stable pulse
-0.52	no pulse

3.4 CRT & Video Adjustments

SETUP

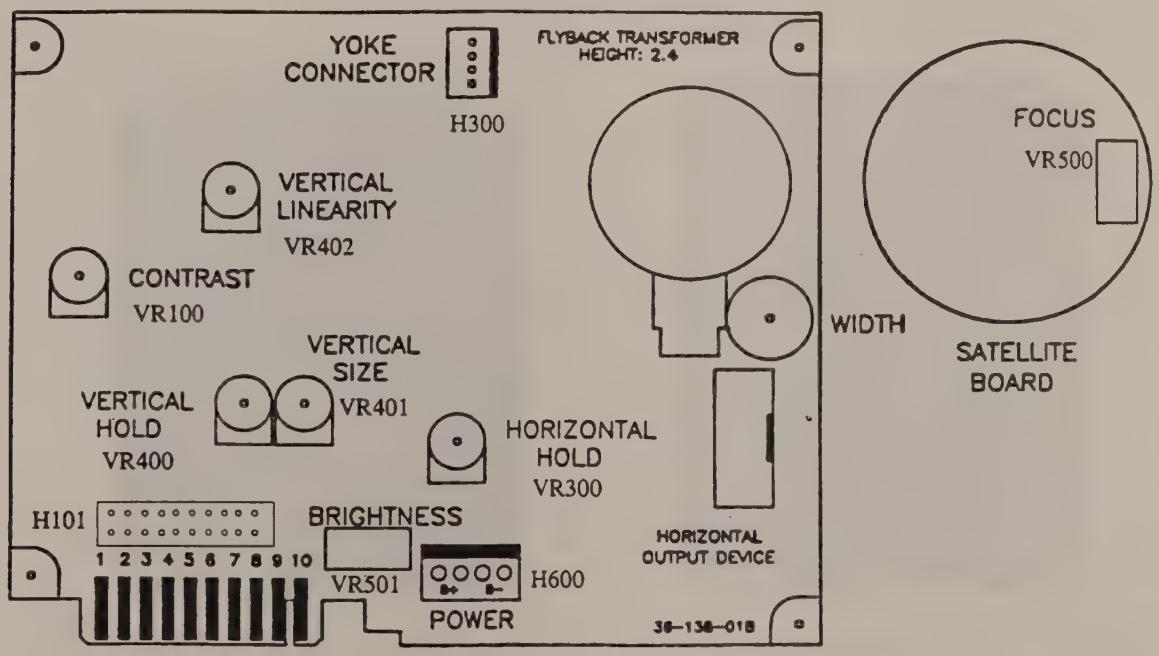
1. Power the instrument on and allow a 15 minute warm-up period.

3.4.1 Horizontal And Vertical Hold Adjustment

NOTE ***Due to the CRT's orientation in this instrument, the Horizontal adjustment effects the vertical display and the Vertical adjustment effects the horizontal display.***

1. Adjust the Horizontal display using VR400 VERTICAL HOLD (see F3.4.). Adjust VR400 clockwise until the display starts to scroll horizontally to the left, then adjust VR400 counter-clockwise until the display starts to scroll horizontally to the right. Adjust VR400 clockwise to the midpoint of the left and right scrolling positions.

2. Adjust the Vertical display using VR300 HORIZONTAL HOLD (see F3.4.). Adjust VR300 clockwise until the display starts to scroll vertically downward, then adjust VR300 counter-clockwise until the display starts to scroll vertically upward. Adjust VR300 clockwise to the midpoint of the downward and upward scrolling positions.



F3.4 Video Display PC Board

3.4.2 Contrast And Brightness Adjustment

1. Set the Brightness level.
   *Press the **MORE** key.*
   *Select **CONFIG** and press the **ENTER** key.*
   *Select **BRIGHT** and adjust for a level of **16** using he inner fine control kob.*

2. Adjust VR501 (Video Brightness, see F3.4.) counter-clockwise until the Display Background becomes just visible as shown in F3.4.2..

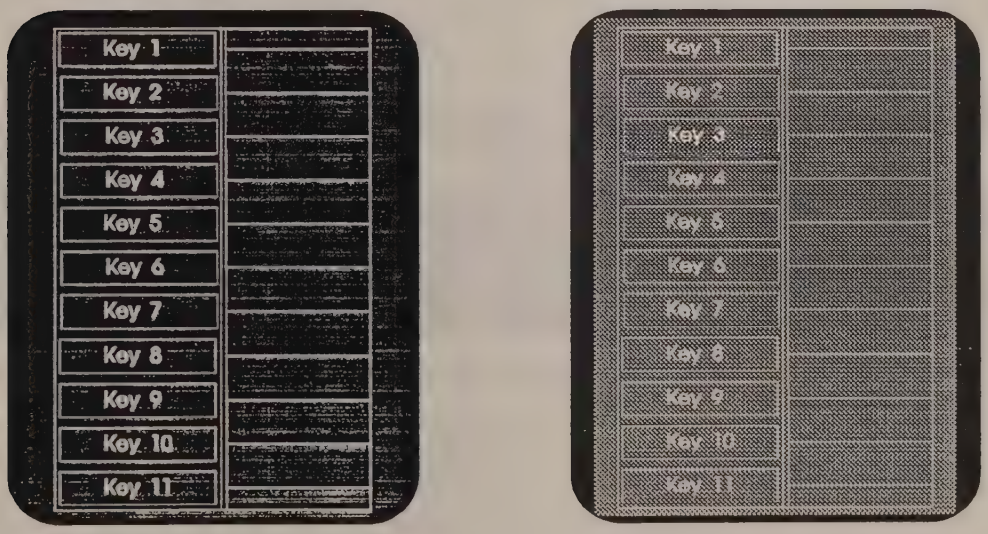
3. Adjust VR100 (Video Contrast, see F3.4) until the displayed text achieves maximum clarity as shown in F3.4.2.3.

4. Adjust VR501 (Video Brightness, see F3.4) slightly counter-clockwise until the Display Background is no longer visible.

5. Check the Brightness.
   *Press the **MORE** key.*
   *Select **CONFIG** and press the **ENTER** key.*

   *Rotate the Inner Fine Control Knob from **16** to **1**. Check that the screen is barely visible, **Brightness level 1 is the result when Screen Save is active.***

   Rotate the Inner Fine Control Knob to set the Brightness at level 12 when check is complete.



No Display Background

Display Background present

F3.4.2 CRT With Display Backround

3.4.3 Display Background Adjustment

SETUP

1. Select the Touch Screen Test screen.
   *Press the **MORE** key.*
   *Select **TEST***
   *Select **TCHTEST***

ADJUSTMENTS

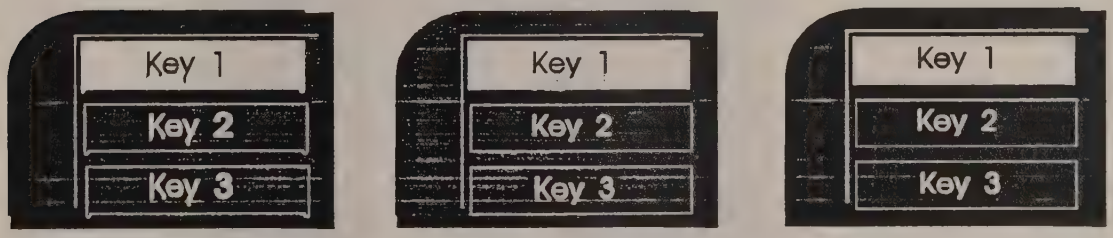
WARNING ***The following adjustment is a very difficult alignment. It should only be attempted by an experienced technician due to the proximity of HIGH VOLTAGE. The instrument has been factory set and should be readjusted only if absolutely necessary.***

1. Carefully adjust the CRT Alignment Tabs (see F3.4.3.2A), located on the CRT, until the Display Background is centered on the CRT. It may be necessary to go back and forth, shown in F3.4.3.2.

2. Adjust VR501 (Video Brightness, see F3.4.) counter-clockwise until the Display Background becomes just visible as shown in F3.4.2.

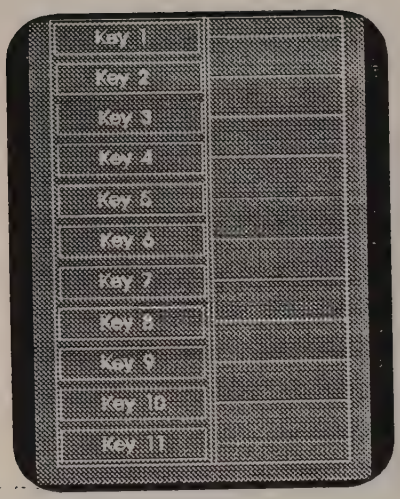
3. Adjust VR300 HORIZONTAL HOLD (see F3.4.) until the Touchscreen Test is centered on the Display Background as shown in F3.4.3.1.

4. Adjust VR501 (Video Brightness, see F3.4) slightly counter-clockwise until the Display Background is no longer visible.



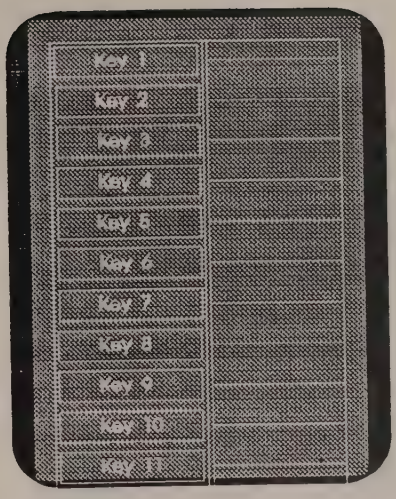
WRONG	WRONG	RIGHT
Text is bleeding.	Text has a shadow.	Clear text

F 3.4.2.3 Effect of Contrast on Text



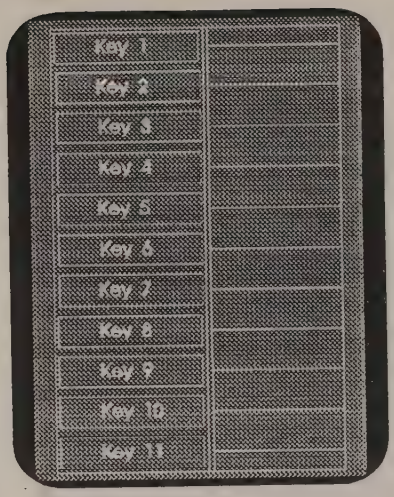
Wrong

Text too high on
Display Background



Wrong

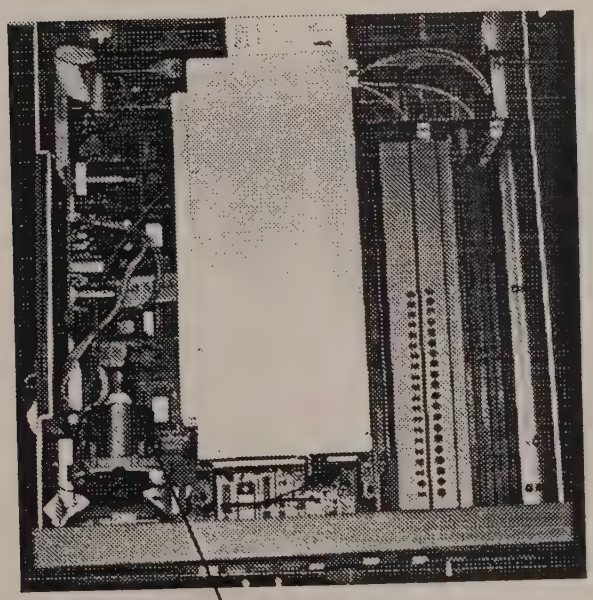
Too low on
Display Background



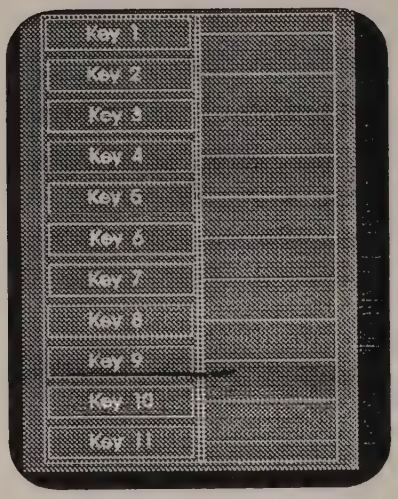
Right

Text Properly Aligned
with Display Background

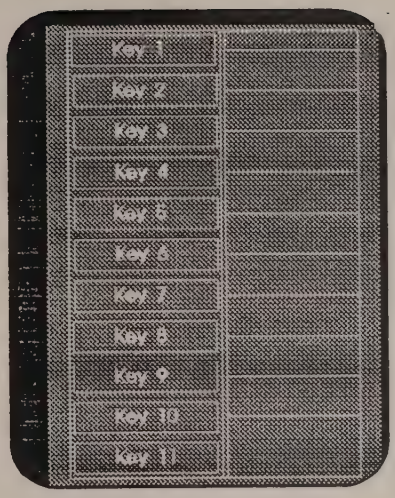
F3.4.3.1 Centering Touch Screen Test on Display Background



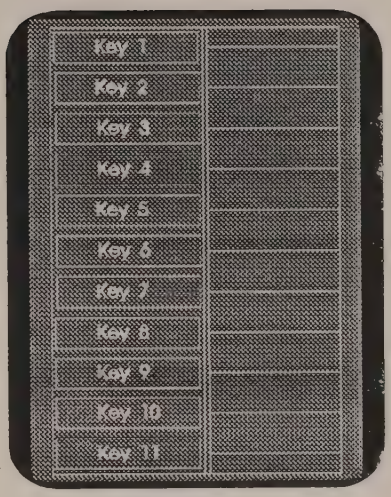
F 3.4.3.2A Location of CRT Alignment Tabs



WRONG



WRONG



RIGHT

F3.4.3.2 Display Background Adjustment Examples

4.0 General Description

The 9210 Pulse Generator is separated into two major functional groups. The Main board (9210main), and the Output module(s).

The Main board, in addition to consisting of Control, Measurement and Timing generation circuitry for both channels, is the primary means of interconnecting the various subsystems that make up the 9210. Figure 4-1, 9210 Block Diagram, shows how the various functions are connected into the Main board.

4.1 Power Supply

The Power Supply is a self-contained, synchronized switching power supply. It will accept AC input voltages from 115 to 220 Volts, 48 to 448 Hertz and will sense and automatically adjust to the input line conditions. A 100 KHz reference frequency (0 to 5 V CMOS logic swing) is provided by circuitry on the Main board in order to synchronize the switching frequency of the supply to a sub-multiple of the microprocessor clock. This was done in order to keep the interference terms generated by the supply consistent from supply to supply.

A logic signal, REMOTE_DISABLE, is provided that allows the DC outputs from the supply to be turned off. One supply (+5B) remains active to provide power to the circuitry that senses the front panel POWER switch. This supply is only turned OFF by either unplugging the power cord from the AC outlet or turning the REAR PANEL Main Circuit Breaker to the OFF position.

The Power Supply provides power to the Main board as well as both modules. The current available on each supply and its allocation is shown below:

SUPPLY	CURRENT AVAIL	MAIN BOARD	MODULE A	MODULE B
+24.0	1.0 AMPS	0.150 AMPS	0.425 AMPS	0.425 AMPS
+15.0	2.5 AMPS	1.000 AMPS	0.750 AMPS	0.750 AMPS
+ 5.0	6.0 AMPS	2.000 AMPS	2.000 AMPS	2.000 AMPS
- 5.2	8.0 AMPS	5.000 AMPS	1.500 AMPS	1.500 AMPS
-15.0	1.2 AMPS	0.200 AMPS	0.500 AMPS	0.500 AMPS
-24.0	1.5 AMPS	0.150 AMPS	0.675 AMPS	0.675 AMPS

4.1.2 Video Sweep Board

The Video Sweep board accepts the Horizontal Sync, Vertical Sync composite video and power from the Main board and generates the voltages and other appropriate signals to drive the CRT.

WARNING!!! WARNING!!! WARNING!!! WARNING!!! WARNING!!! WARNING!!!

There are dangerously high voltages present on the Video Sweep board and on the RED cable connecting the Sweep board to the CRT. Exercise EXTREME caution when operating the unit with the cover removed !

4.1.3 Front Panel Board

The Front Panel board consists of the components required to implement the user interface. These are the Keypad, Touch CRT LEDs and detectors, GPIB Status LEDs, Coarse and Fine knobs and the POWER switch. There is some current buffering on the Front Panel board to drive the Touch CRT LEDs. (See block Diagram, F4-1-1).

All the control signals originate from the 9210 main board. The Front Panel scan Timing diagram, F4-1-2, shows the timing of the scan signals after a microprocessor RESET or POWER ON. The Keypad is scanned by driving the rows LOW, one at a time, and reading the pattern present on the column lines. Pressing a key shorts a specific row to a specific column and this pattern is decoded by the Front Panel microcontroller on the 9210 main board. F4-1-3, Key Scan Table, shows the row and column connections for each key in the matrix. Note that the module Front panel keys are included in the matrix. Also note that the module is detected as being "IN PLACE" using the Key Scan matrix.

The Touch CRT Keys function in a similar manner. The LED is driven and the detector is sensed. If the detector does not get turned ON by the LED it is assumed to be blocked and hence selected. The selected Touch CRT key closest to the TOP of the screen will always take precedence if more than one field is selected. Since the field is selected by virtue of the detector NOT responding, high ambient light conditions can saturate the detector and cause the Touch CRT system to malfunction.

As described above in the POWER SUPPLY section, the Front Panel POWER switch DOES NOT remove AC power from the unit. It simply disables most of the DC outputs from the supply. AC power can only be safely removed by disconnecting the power cord from the AC line.

4.1.4 Module Interconnections

There are various connections from the 9210 main board to the backplane containing the module connectors. Most of the connections are digital busses or control lines. These lines are routed through a 60 pin header that connects to the backplane board which in turn connects to the module connectors (Refer to 9210 Block Diagram F4-1). There are also three coaxial cables that connect directly from the 9210 main board to the module connector. These carry critical high frequency signals to the module and the timing readback signal from the module.

The pulse is created on the 9210 main board to have the correct DELAY from trigger and WIDTH. The outputs from the main board are DIFFERENTIAL ECL logic signals. These are the signals shown as CHANNEL (A or B) PULSE OUT on the block diagram. They are source terminated 50 ohm transmission lines as they leave the 9210 main board and are also terminated at the end of the transmission line on each module in order to minimize pulse distortions due to line impedance mismatches. The amplitude, offset and transition time (when applicable) are module functions and are discussed later in the section containing the module descriptions.

The other coaxial cable from each module is the Timing Readback. It is used during calibration and allows parameters such as transition time, pulse width or other timing measurements to be made directly on the OUTPUT of the module. The specific use of this signal in each module will be discussed in the section for that module. It is also a doubly terminated 50 ohm transmission line.

4.1.5 Other Connections

Other connections to the Main board are the two fans and the GPIB connector on the rear panel. The fans connect to a temperature sensing circuit that controls their speed. The GPIB connector is mounted to the rear panel and connected to its appropriate control signals on the Main board by a short ribbon cable.

4.2 General Description

Refer to 9210 main block diagram, F4.2. The 9210 main board is comprised of 7 major functional areas. They are as follows:

1) Microprocessor (F4.2.1)
2) Video Controller (F4.2.2)
3) GPIB Interface (F4.2.3)
4) Front Panel Interface (F4.2.4)
5) Measurement & Calibration (F4.2.5)
6) Trigger Processing & Period Generation (F4.2.6)
7) Delay & Width Generation (F4.2.7)

The block diagram shows how these major functions interconnect. Each block breaks out into a more detailed block diagram as well as showing the 9210 main schematic page(s) that detail the circuitry. The schematic diagrams can be found in Section 7, Schematics.

Using this heirarchical approach along with the following descriptions it should be relatively straightforward to gain a basic understanding of the inner workings of the Pulse Generator.

The majority of the functionality of the Pulse Generator exists in the custom designed ASIC called the MTG301. This IC is basically a triggerable VCO based delay generator. The delay is a function of the VCO period and the number of VCO cycles allowed to complete. For example, a delay of 100 ns can be obtained by setting the VCO to 6.25 ns period and counting 16 VCO cycles (16 * 6.25 ns = 100 ns). This delay can be changed to be 100.1 ns by changing the VCO frequency to 6.256 ns. The VCO control voltage (or more strictly control current in this case) is set by a 14 bit DAC.

In order to implement a period generator, the VCO is allowed to free run. A width is generated by setting a flip-flop upon receipt of a trigger and resetting the flip-flop at the end of the delay time.

The VCO of each of the MTGs in the system is calibrated at a number of DAC codes. This is accomplished by setting a DAC code for the particular VCO and measuring its frequency. The frequency is measured by gating a VCO divided by 64 frequency to the FCAL

4.2 General Description

Refer to 9210 main block diagram, F4.1. The 9210 main board is comprised of 7 major functional areas. They are as follows:

1) Microprocessor (F4.2.1)
2) Video Controller (F4.2.2)
3) GPIB Interface (F4.2.3)
4) Front Panel Interface (F4.2.4)
5) Measurement & Calibration (F4.2.5)
6) Trigger Processing & Period Generation (F4.2.6)
7) Delay & Width Generation (F4.2.7)

The block diagram shows how these major functions interconnect. Each block breaks out into a more detailed block diagram as well as showing the 9210 main schematic page(s) that detail the circuitry. The schematic diagrams can be found in Section 7, Schematics.

Using this heirarchical approach along with the following descriptions it should be relatively straightforward to gain a basic understanding of the inner workings of the Pulse Generator.

The majority of the functionality of the Pulse Generator exists in the custom designed ASIC called the MTG301. This IC is basically a triggerable VCO based delay generator. The delay is a function of the VCO period and the number of VCO cycles allowed to complete. For example, a delay of 100 ns can be obtained by setting the VCO to 6.25 ns period and counting 16 VCO cycles (16 * 6.25 ns = 100 ns). This delay can be changed to be 100.1 ns by changing the VCO frequency to 6.256 ns. The VCO control voltage (or more strictly control current in this case) is set by a 14 bit DAC.

In order to implement a period generator, the VCO is allowed to free run. A width is generated by setting a flip-flop upon receipt of a trigger and resetting the flip-flop at the end of the delay time.

The VCO of each of the MTGs in the system is calibrated at a number of DAC codes. This is accomplished by setting a DAC code for the particular VCO and measuring its frequency. The frequency is measured by gating a VCO divided by 64 frequency to the FCAL

bus (an ECL emitter ORed bus) which is measured by the frequency counter inside the PVC302. The ability to gate the prescaled VCO frequency onto the FCAL bus is built into the MTG IC and is invoked under microprocessor control.

The MTG only has 9 bits of counter built into it. Therefore, in order to achieve long times external counters are required. These counters are built into an FPGA called the PCT303. Each MTG has 16 bits of additional counter in the PCT303 for a total of 25 bits of counter.

4.2.1 Microprocessor (Block Diagram F4.2.1)

The microprocessor is a Motorola 68008. Along with the 68901 Multi Function Peripheral and RAM and PROM it forms the core microprocessor control section of the 9210 main board.

All the control circuitry in the Pulse Generator, such as DACs and control registers are memory mapped. That is, they are addressed in the microprocessor's memory space in the same manner as RAM would be. One significant point regarding the 68008 is that it implements asynchronous bus timing. This means that a microprocessor READ or WRITE cycle is completed up to a point and then operation is suspended until a handshake signal (DTACK - Data Transfer Acknowledge) is received. The result is that microprocessor bus cycles can be held in a specific state for as long as it takes the addressed peripheral to obtain valid data. It also requires that every decoded address generate a DTACK signal or the microprocessor will "hang up" forever.

For the core microprocessor circuitry, a PAL generates the DTACK signal. The Video controller generates its own DTACK signal and the PCT303 Counter/Decoder FPGA (Field Programmable Gate Array) decodes addresses and generates the DTACK signal for the rest of the system, including the modules. The DTACK bus is a pulled up open collector type bus. This means it is either driven to a low logic level or open, in which case it is pulled up to a logic high through a resistor.

In order to control the microprocessor's behavior during power up and power interruption times and to keep the microprocessor from "hanging up" indefinitely, a supervisor circuit is included on the board. It monitors the power supply voltage and must be triggered by the microprocessor a minimum of approximately once per second. If anything is wrong, it RESETS the system, including the microprocessor.

4.2.2 Video Controller (Block Diagram F4.2.2)

The Video Controller is an FPGA (Field Programmable Gate Array). It is called the PVC302. In addition to handling all the timing and control of the video circuitry, it provides a frequency counter (used by the calibration system) and some interface circuitry between the Measurement system and the microprocessor.

The Video memory consists of a Bit Map RAM (any pixel on the screen can be turned ON or OFF -- used for displaying graphics) and a Character RAM. Actually, both these functions are in the same physical RAM and the Video Controller takes care of getting the correct data from the RAM at the correct time. The Video Controller also handles the task of looking up the correct pixel data for each scan line of each character in the FONT PROM.

The Video memory is in the microprocessor's address space and the microprocessor can READ or WRITE RAM data at any time. However, the Video controller does not provide a DTACK signal to the microprocessor, therefore not allowing the bus cycle to complete, until the RAM is not being used by the Video system. This delay could be as much as 4 microseconds for each byte written. This is significantly less than if the microprocessor were only allowed to access the RAM during CRT retrace times and still allows the display to be free of "noise".

The display is capable of displaying 11 lines of 18 characters each. The graphics resolution is 318 X 640. The CRT is turned sideways so the 640 points are from the top to the bottom of the CRT. The control signal frequencies are as follows :

Pixel Rate	**16.00 MHz (500 nS/point)**
Horiz Sync Rate	**21.98 KHz (45.5uS)**
Horiz Sync Width	**4.5uS**
Vert Sync Rate	**57.09 Hz (17.52mS)**
Vert Sync Width	**682.5 uS**

4.2.3 Gpib Interface (Block Diagram F4.2.3)

The GPIB interface is comprised of three ICs. A 9914 GPIB controller, and two GPIB bus buffers. The 9914 handles the GPIB protocol and communicates with the microprocessor by interrupting it and the microprocessor services the interrupt accordingly. The bus buffers drive and receive data directly from the outside world through the GPIB connector. They are socketed for ease of replacement in the event that they are damaged by an external fault on the GPIB bus.

4.2.4 Front Panel Interface (Block Diagram F4.2.4)

The Front Panel interface is controlled by a 68705 microcontroller. It implements the Front Panel scan and interprets the results. When it needs to communicate with the main microprocessor, it places data in a latch and generates an interrupt to the main microprocessor. After the main microprocessor takes the data, it sends an interrupt to the front panel microcontroller to signify that the transfer is complete. The version of the 68705 that is used in the Pulse Generator contains an 8 bit A/D converter. This is used to determine the position of the front panel COARSE and FINE knobs. See the section on the Front Panel Board and its associated block diagram (F4.1.1).

4.2.5 Measurement & Calibration System (Block Diagram F4.2.5)

The Measurement system consists of most of the circuitry required to measure various timing parameters and voltages in the unit so that circuits may be tested and "tweaked" to yield the very high degree of accuracy specified for the unit. The one significant function that is not physically in the same area as the rest of the measurement circuitry but is part of the measurement system is the frequency counter. It is in the Video controller FPGA (PVC302). The output of the TDC Start Mux is level shifted from ECL to TTL and routed to the PVC302. Refer to the block diagrm of the Measurement System.

The timing readback from each module is connected to a very high speed comparator. The other input to the comparator is connected to a DAC that allows the comparison voltage, or comparator threshold, to be set to any voltage between ±2.5 Volts with approximately 20 mV resolution. This feature is used to measure the rise and fall times of the module output. The threshold can be set to the 10% point on the pulse and, using the TDC, the time from a trigger to the comparator threshold crossing is measured. Then the threshold is set to the 90% point on the pulse and the time from the same trigger to the comparator threshold crossing is measured. The time difference is the 10%-90% rise time. This basic sequence is repeated many times depending upon which module is installed.

The TDC Start and Stop muxes are ECL muxes that route, under microprocessor control, which signal starts and stops the TDC. When the TDC is started, a ramp is started. When the TDC Stop is received the ramp is stopped and held at whatever voltage it has achieved. A TDC stop signal is sent to the PVC302 and also interrupts the microprocessor. The PVC302 causes the A/D to read the held voltage so a 12 bit digital representation of the

time from start is available to the microprocessor. The resolution of the TDC is approximately 20 ps/code. All readings are averaged, and the noise is random, so the effective resolution is much better than 20 ps.

The A/D is used to measure various other voltages to calibrate DC characteristics of the modules through the module voltage readback signals. It is also used to measure the thermal diode chain which effectively measures the average chip temperature of the timing generation ICs (MTGs).

The temperature change of the timing generation ICs is monitored and small corrections in the control current are made in order to compensate for the timing drift of approximately 7 ps/ °C. This function can be disabled by turning TempComp to OFF via a Front Panel menu selection.

4.2.6 Trigger Processing & Period Generation (Block Diagram F4.2.6)

The trigger/period circuitry is comprised of the trigger input and output signal conditioning, protection circuitry and period generator MTG. The function of the circuitry is to select the trigger threshold, trigger mode, trigger slope, set the period (if required in the selected trigger mode) and program the BURST count in BURST mode. The input signal is attenuated and limited for protection. The attenuated signal is then applied to a comparator. The output from the comparator is applied to the trigger input of the MTG. Trigger slope, trigger mode and period are all selected inside the MTG. Burst count is inside the MTG for periods less than 19 ns and in the PCT303 for periods greater than 19 ns. The trigger output pulse width is determined by the selected trigger mode. In GATE mode, for example, the trigger output width is the same as the gate input. In NORMAL mode, the trigger output from the MTG varies from ≈3.6 ns to ≈7.2 ns. A trigger stretch circuit exists to make the output trigger longer by ≈20 ns for requested periods of greater than 40 ns. The trigger stretch circuitry is also activated in SINGLE trigger mode. It is switched in when the requested WIDTH is greater than 40 ns. Finally, the ECL logic level is shifted and applied to a driver stage capable of driving a 50 ohm load. The voltage swing at the output is nominally 1 Vp-p into 50 Ω. The offset is programmable to ± 1.5V into 50 Ω.

The period generator MTG outputs a separate differential ECL trigger pulse for Channel A and Channel B. The width outputs from the period generator are sent to the measurement system so that the trigger frequency can be measured and reported in single trigger mode. One output is direct and the other is divided by 10 so that the counter will work all the way to 300 MHz.

4.2.7 Delay & Width Generation (Block Diagram F4.2.7)

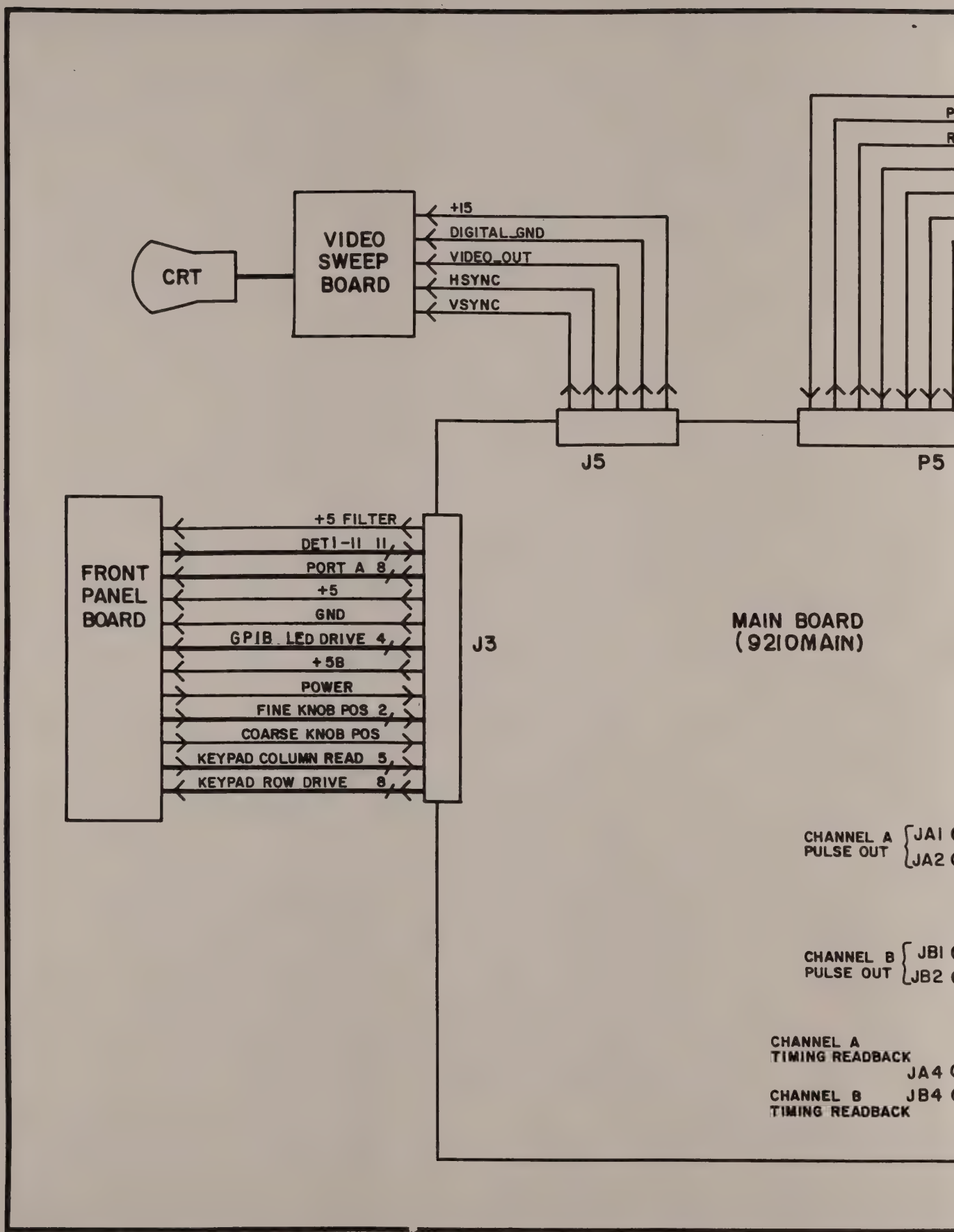
The circuitry for the Delay and Width generation is essentially the same for both channels. The main difference is that the thermal diode in the channel B width generator is not connected in the chain. The fact that it is not connected does not materially alter the operation of the temperature compensation.

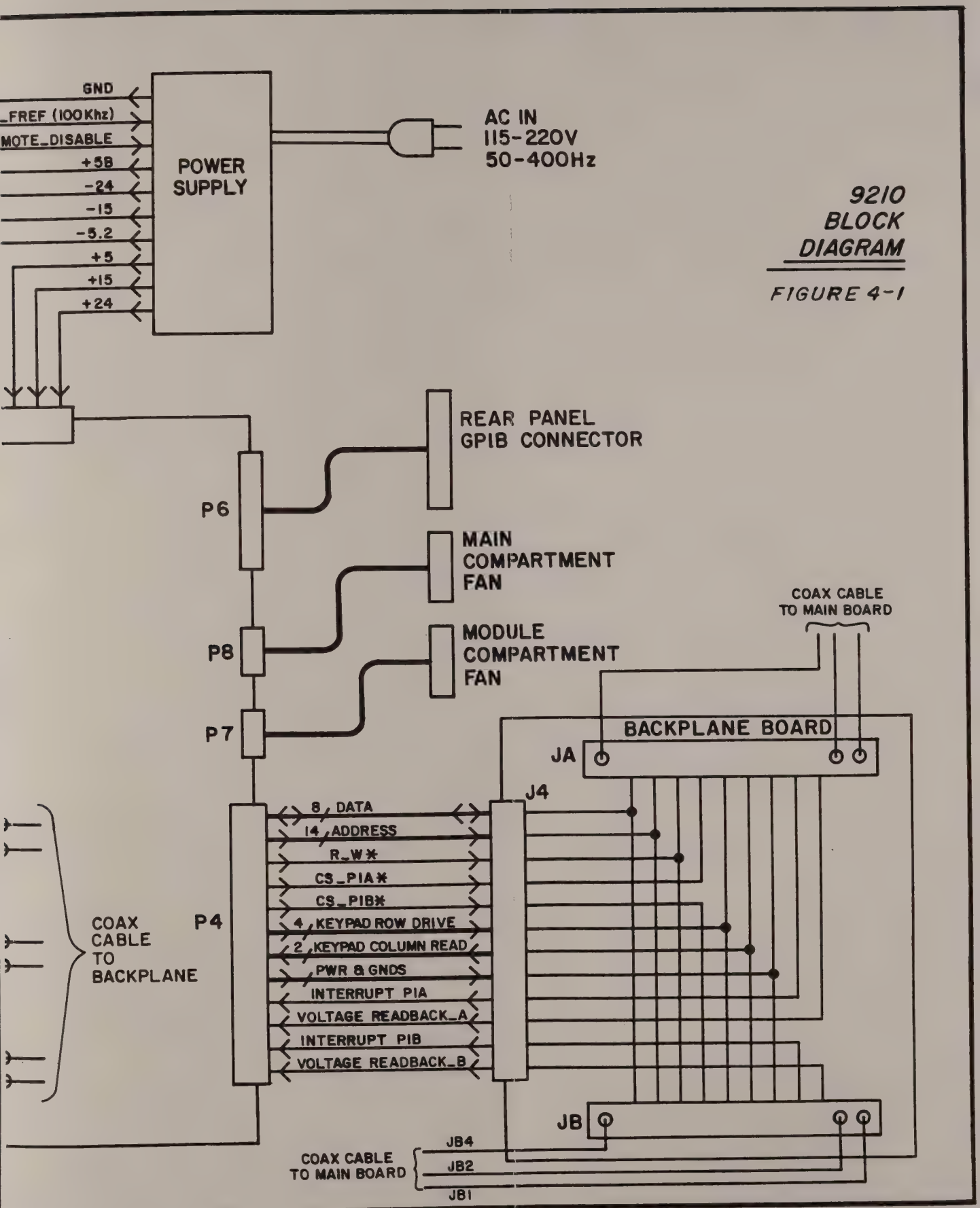
A trigger is received from the period generator into the delay generator. After the delay time elapses, a pulse is output from the delay generator to trigger the width generator. This pulse is a differential ECL signal that is approximately 1.2 ns wide. Therefore it will be very difficult to see on an oscilloscope at long periods.

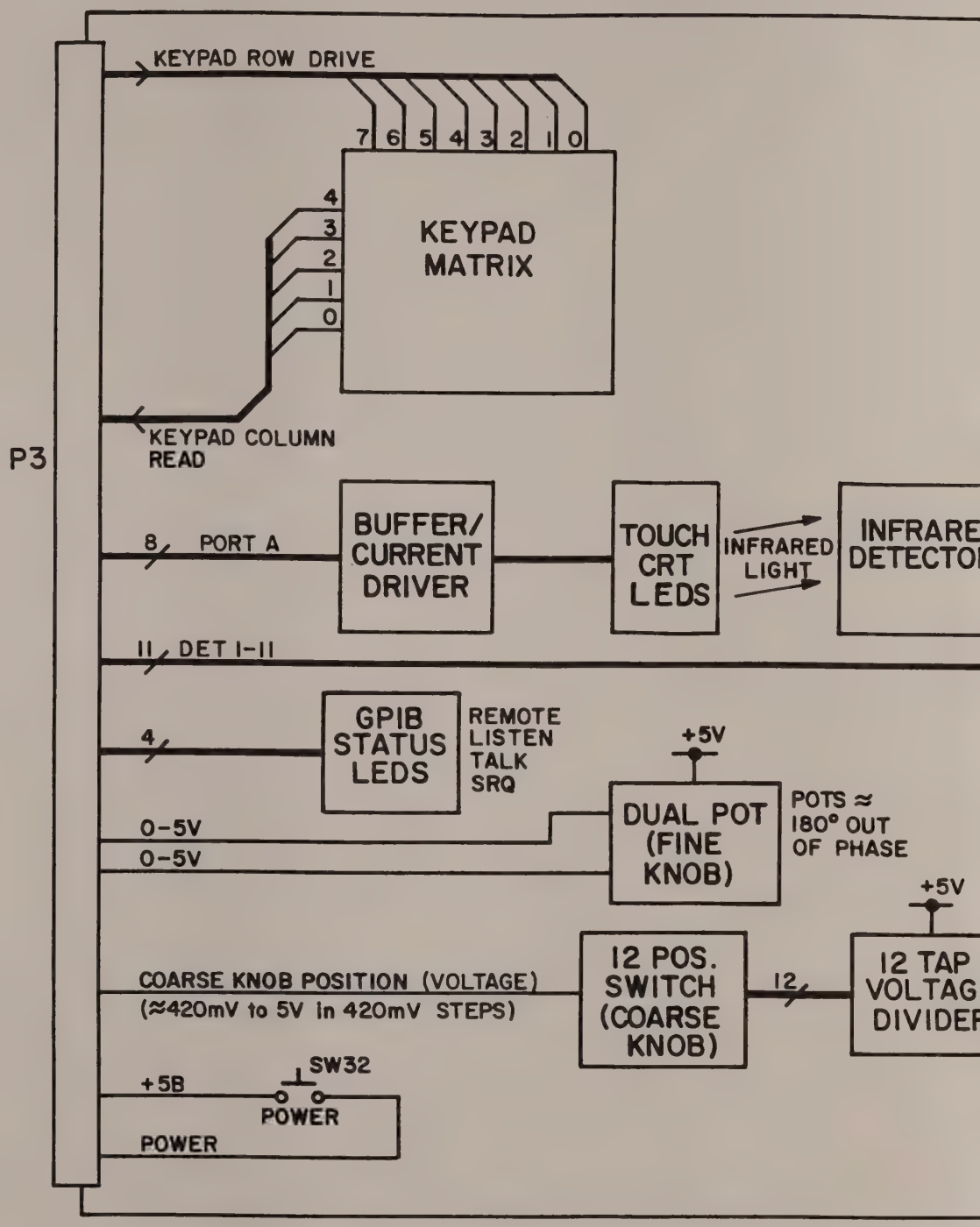
The trigger input pulse to the delay generator is also a narrow pulse. In double pulse mode, the trigger pulse is gated to the output of the delay generator in addition to the "end of delay" pulse. This causes two triggers into the width generator. One at "zero" delay and one at the programmed delay.

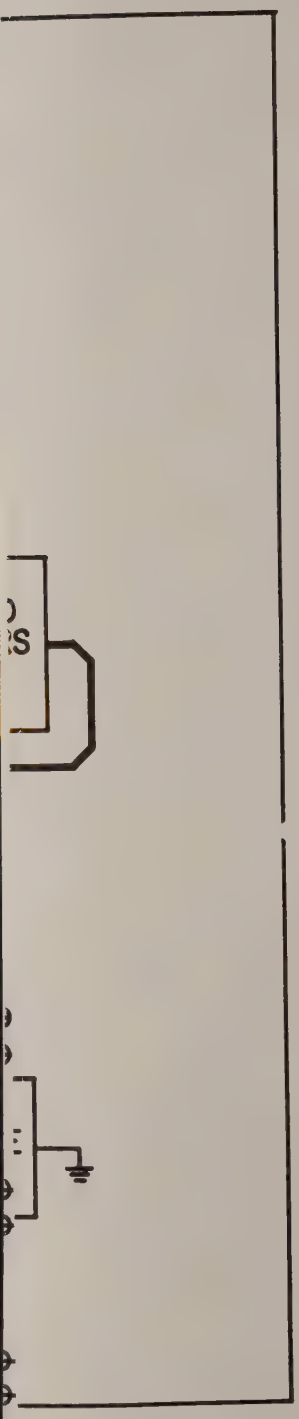
When the width generator is triggered, its width output is set to a logic one. After the programmed time elapses, the output is reset to a logic zero. In this manner the output width is generated.

It should be noted again here that the MTG is a custom designed ASIC and that the particular function of the IC is determined under program control. In other words, all the MTGs are the same IC with different programming to achieve the desired function. Also, the MTGs are socketed so that they can be relatively easily changed.


CRT
VIDEO SWEEP BOARD
+15
DIGITAL_GND
VIDEO_OUT
HSYNC
VSYNC
J5
P5
FRONT PANEL BOARD
+5 FILTER
DET1-11 11
PORT A 8
+5
GND
GPIB_LED DRIVE 4
+5B
POWER
FINE KNOB POS 2
COARSE KNOB POS
KEYPAD COLUMN READ 5
KEYPAD ROW DRIVE 8
J3
MAIN BOARD
(9210MAIN)
CHANNEL A PULSE OUT
JA1
JA2
CHANNEL B PULSE OUT
JB1
JB2
CHANNEL A TIMING READBACK
JA4
CHANNEL B TIMING READBACK
JB4

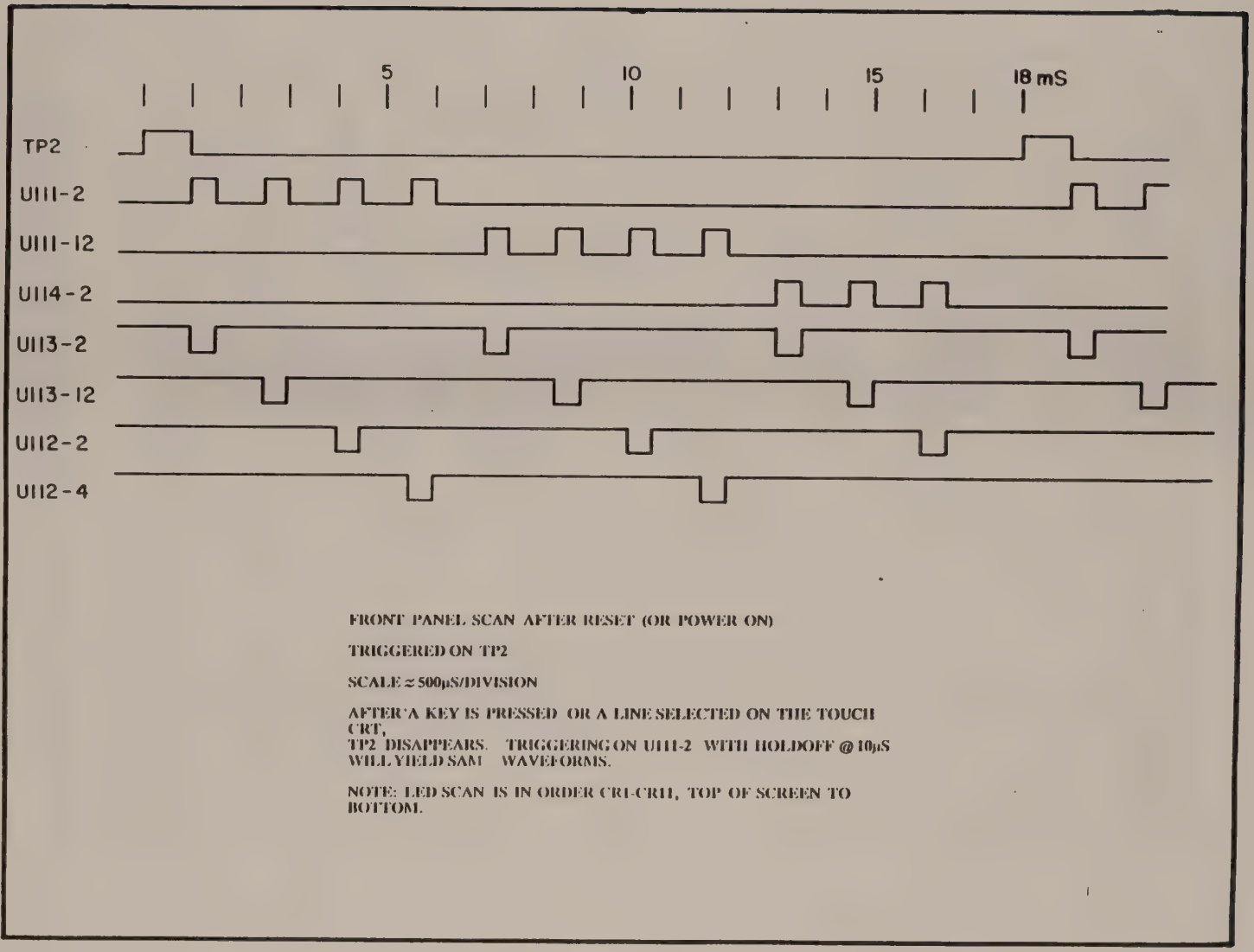

GND
_FREF (100Khz)
MOTE_DISABLE
+5B
-24
-15
-5.2
+5
+15
+24
POWER SUPPLY
AC IN
115-220V
50-400Hz
9210
BLOCK
DIAGRAM
FIGURE 4-1
REAR PANEL
GPIB CONNECTOR
P6
MAIN
COMPARTMENT
FAN
P8
MODULE
COMPARTMENT
FAN
P7
COAX CABLE
TO MAIN BOARD
BACKPLANE BOARD
JA
J4
8 DATA
14 ADDRESS
R_W*
CS_PIA*
CS_PIB*
4 KEYPAD ROW DRIVE
2 KEYPAD COLUMN READ
PWR & GNDS
INTERRUPT PIA
VOLTAGE READBACK_A
INTERRUPT PIB
VOLTAGE READBACK_B
P4
COAX
CABLE
TO
BACKPLANE
JB
JB4
JB2
JB1
COAX CABLE
TO MAIN BOARD


KEYPAD ROW DRIVE
7 6 5 4 3 2 1 0
4
3
2
1
0
KEYPAD MATRIX
KEYPAD COLUMN READ
P3
8 PORT A
BUFFER/ CURRENT DRIVER
TOUCH CRT LEDS
INFRARED LIGHT
INFRARE DETECTO
11 DET 1-11
4
GPIB STATUS LEDS
REMOTE
LISTEN
TALK
SRQ
+5V
DUAL POT (FINE KNOB)
POTS ≈ 180° OUT OF PHASE
0-5V
0-5V
+5V
COARSE KNOB POSITION (VOLTAGE)
(≈420mV to 5V in 420mV STEPS)
12 POS. SWITCH (COARSE KNOB)
12
12 TAP VOLTAG DIVIDER
SW32
+5B
POWER
POWER



FRONT PANEL BOARD
BLOCK DIAGRAM

FIGURE 4-1-1



FRONT PANEL SCAN AFTER RESET (OR POWER ON)

TRIGGERED ON TP2

SCALE ≈ 500μS/DIVISION

AFTER A KEY IS PRESSED OR A LINE SELECTED ON THE TOUCH CRT,
TP2 DISAPPEARS. TRIGGERING ON U111-2 WITH HOLDOFF @ 10μS WILL YIELD SAM WAVEFORMS.

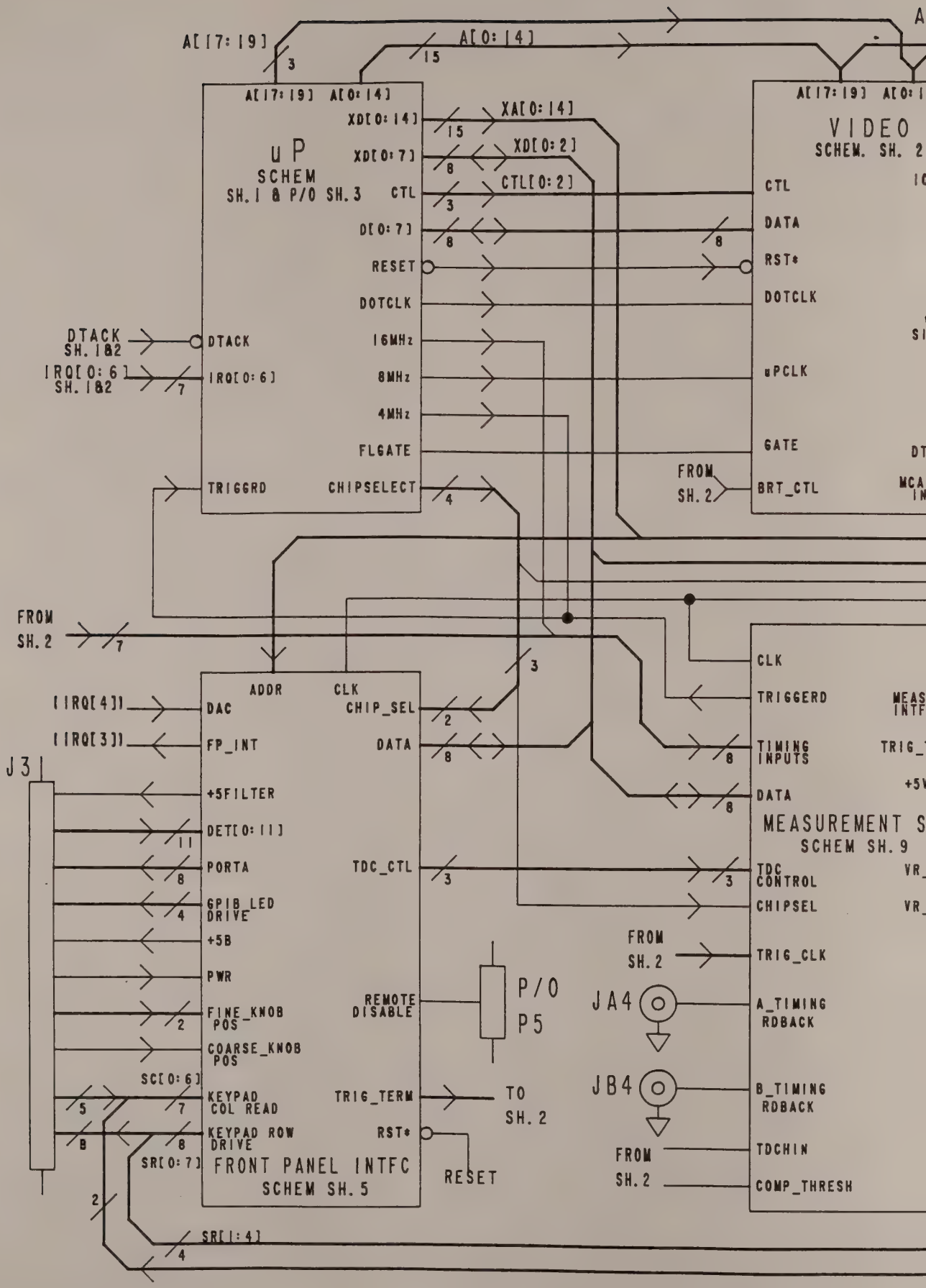
NOTE: LED SCAN IS IN ORDER CR1-CR11, TOP OF SCREEN TO BOTTOM.

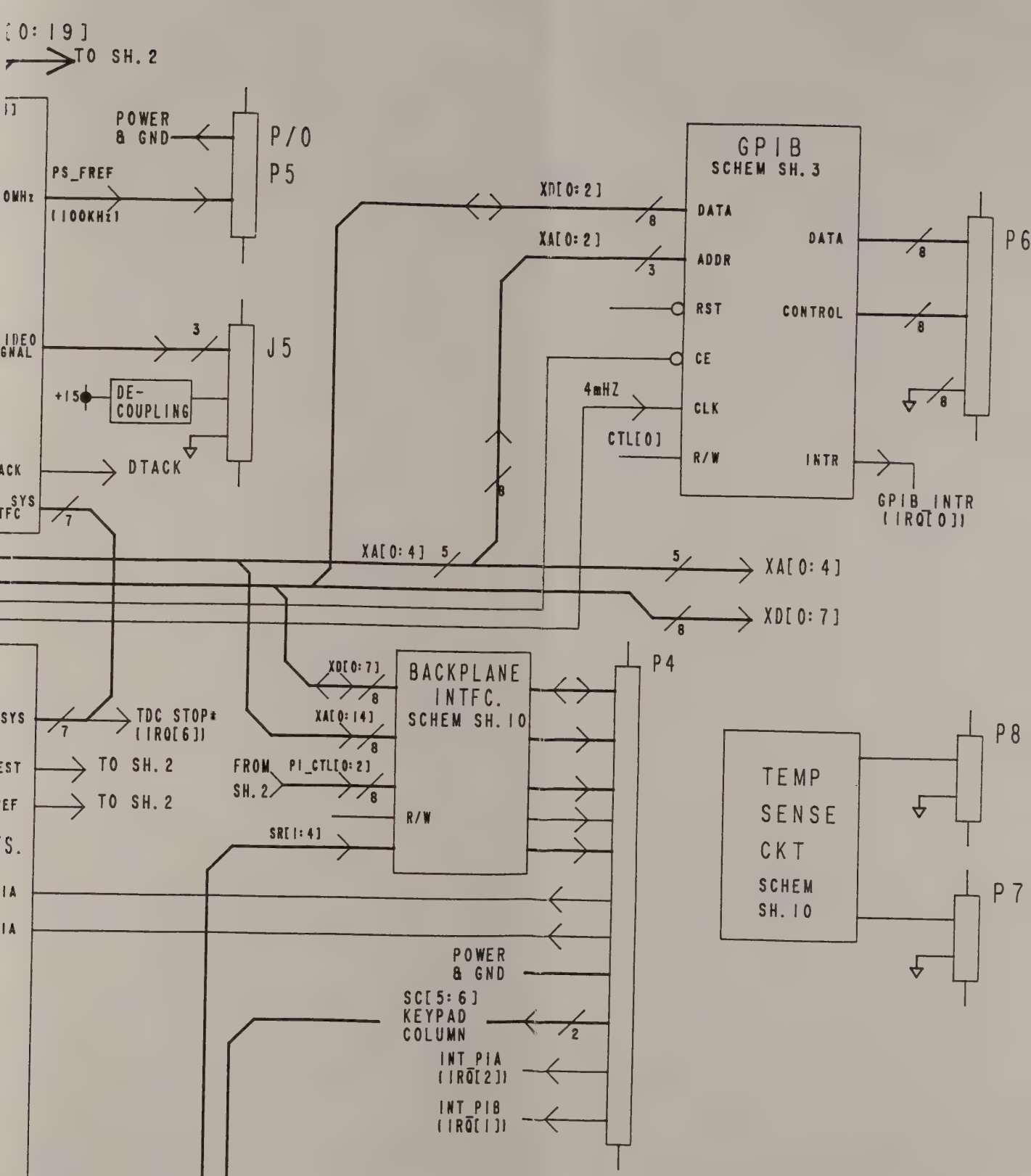
F4.1.2 Front Panel Scan Timing

KEYPAD SWITCH #	FRONT PNL LEGEND	ROW CONNECT.	COLUMN CONNECT.
1	↑	0	0
2	↓	1	0
3	7	2	0
4	4	3	0
5	1	4	0
6	0	5	0
7	MANUAL	6	0
8	CHANNEL A	0	1
9	CHG FORMAT	1	1
10	8	2	1
11	5	3	1
12	2	4	1
13	. (DEC. PT)	5	1
14	9	2	2
15	6	3	2
16	3	4	2
17	+/-	5	2
18	CHANNEL B	0	2
19	MORE	1	2
20	n/Ghz	2	3
21	μ/Mhz	3	3
22	m/Khz	4	3
23	ENTER/Hz	5	3
24	TRIGGER	0	3
25	HELP	1	3
26	STORE SETUP	2	4
27	RECALL SETUP	3	4
28	BACK SPACE	5	4
29	LOCAL	1	4
30	←DIGIT	6	4
31	DIGIT→	7	4
MODULE A	IN PLACE	4	5
	INVERT	3	5
	DISABLE	1	5
	DISP. CHAN.	2	5
MODULE B	IN PLACE	4	6
	INVERT	3	6
	DISABLE	1	6
	DISP. CHAN.	2	6

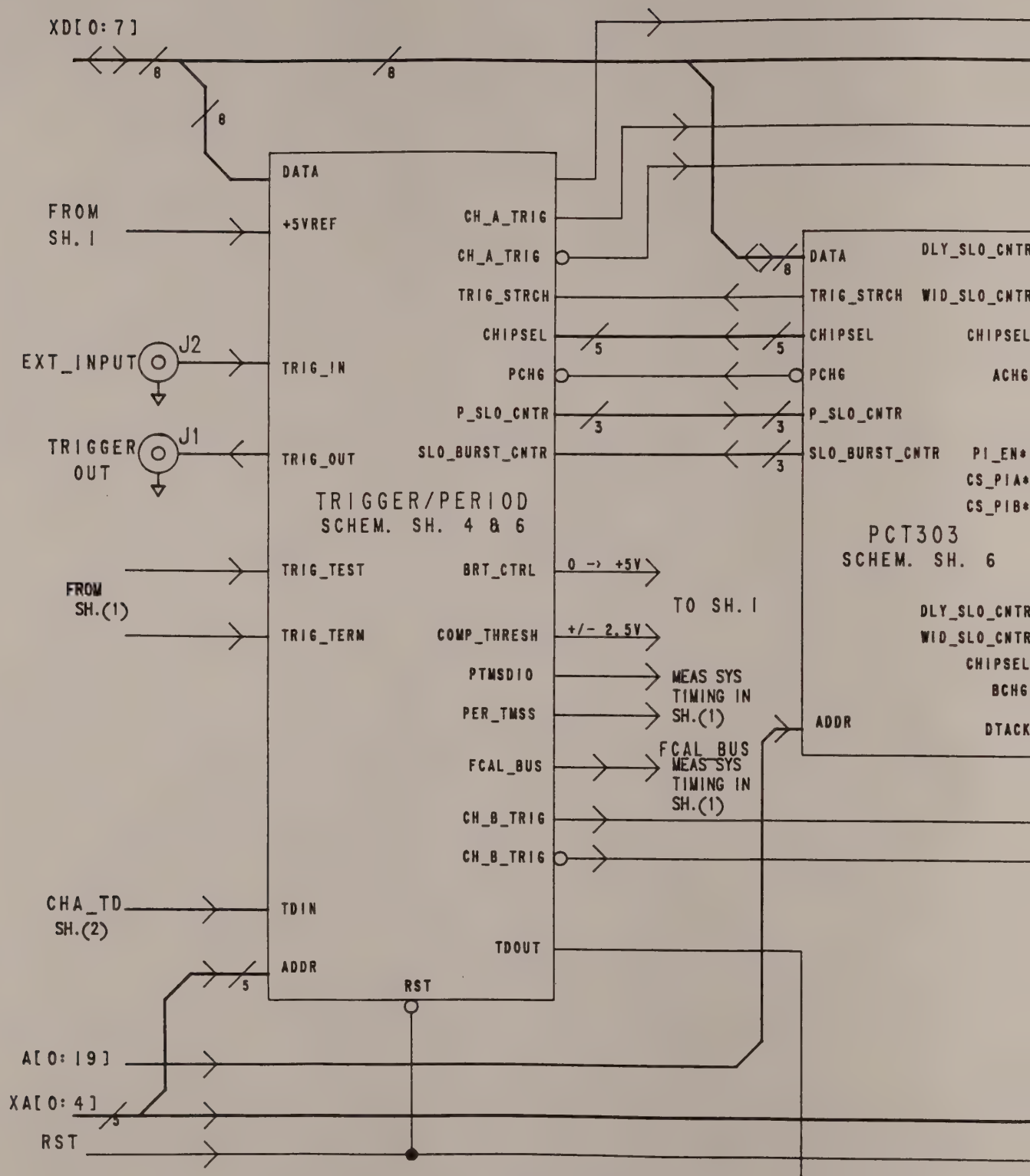
MAINFRAME KEYPAD SWITCH #32 CONNECTS "+5VB" TO "POWER" SIGNALS. NOT PART OF KEYPAD SCAN MATRIX.

F4.1.3 Key Scan Table

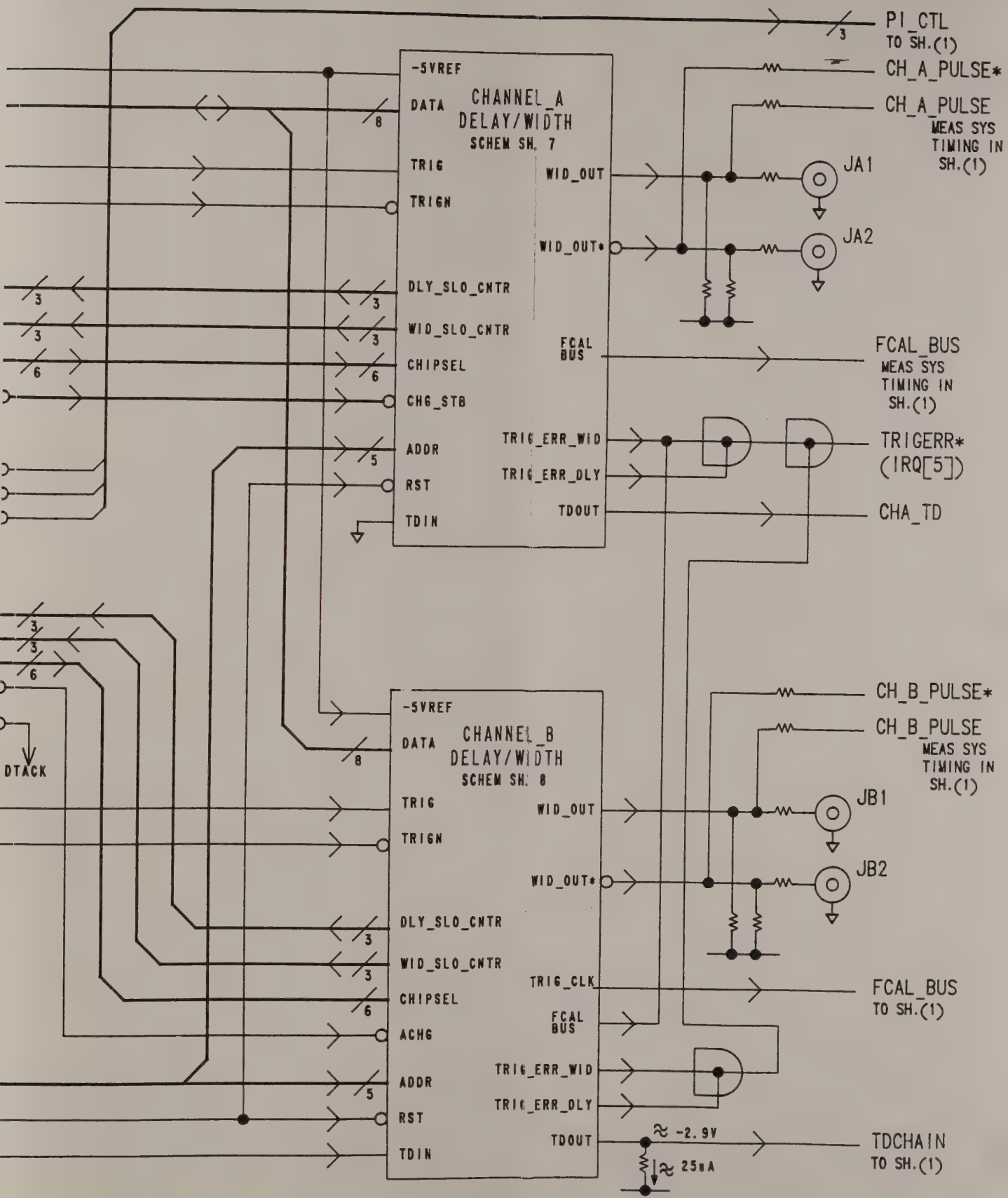

A[7:19]
A[0:14]
uP
SCHEM
SH.1 & P/O SH.3
XD[0:14]
XD[0:7]
CTL
D[0:7]
RESET
DOTCLK
16MHz
8MHz
4MHz
FLGATE
CHIPSELECT
XA[0:14]
XD[0:2]
CTL[0:2]
DTACK
SH.1&2
IRQ[0:6]
SH.1&2
DTACK
IRQ[0:6]
TRIGGRD
VIDEO
SCHEM. SH. 2
CTL
DATA
RST*
DOTCLK
μPCLK
GATE
BRT_CTL
FROM
SH.2
FROM
SH.2
ADDR
CLK
DAC
FP_INT
CHIP_SEL
DATA
[IRQ[4]]
[IRQ[3]]
CLK
TRIGGERD
TIMING
INPUTS
DATA
MEASUREMENT S
SCHEM SH. 9
TDC
CONTROL
CHIPSEL
TDC_CTL
J3
+5FILTER
DET[0:11]
PORTA
GPIB LED
DRIVE
+5B
PWR
FINE_KNOB
POS
COARSE_KNOB
POS
SC[0:6]
KEYPAD
COL READ
KEYPAD ROW
DRIVE
SR[0:7]
REMOTE
DISABLE
TRIG_TERM
RST*
FRONT PANEL INTFC
SCHEM SH. 5
P/O
P5
TO
SH. 2
RESET
FROM
SH.2
TRIG_CLK
JA4
A_TIMING
RDBACK
JB4
B_TIMING
RDBACK
FROM
SH.2
TDCHIN
COMP_THRESH
SR[1:4]

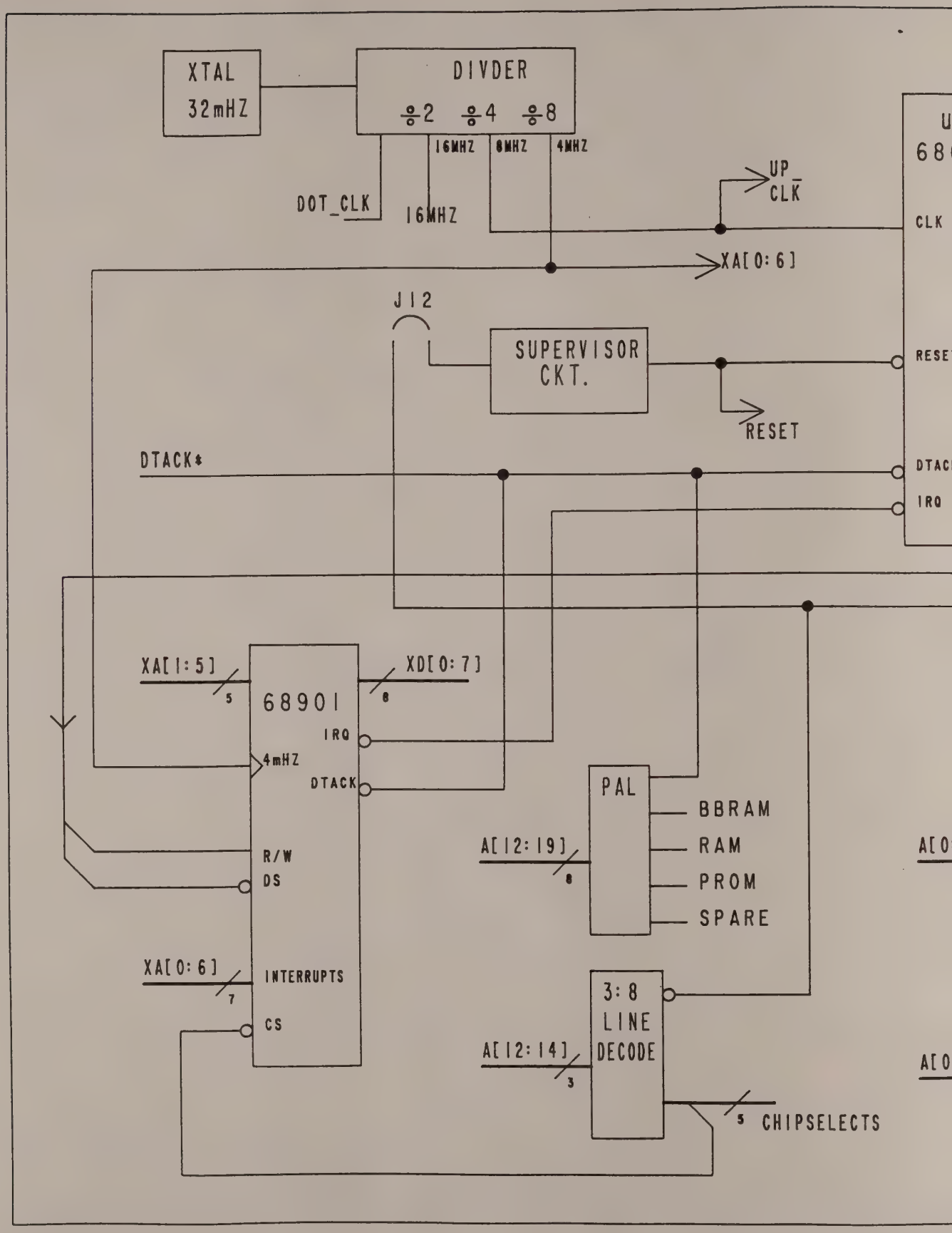


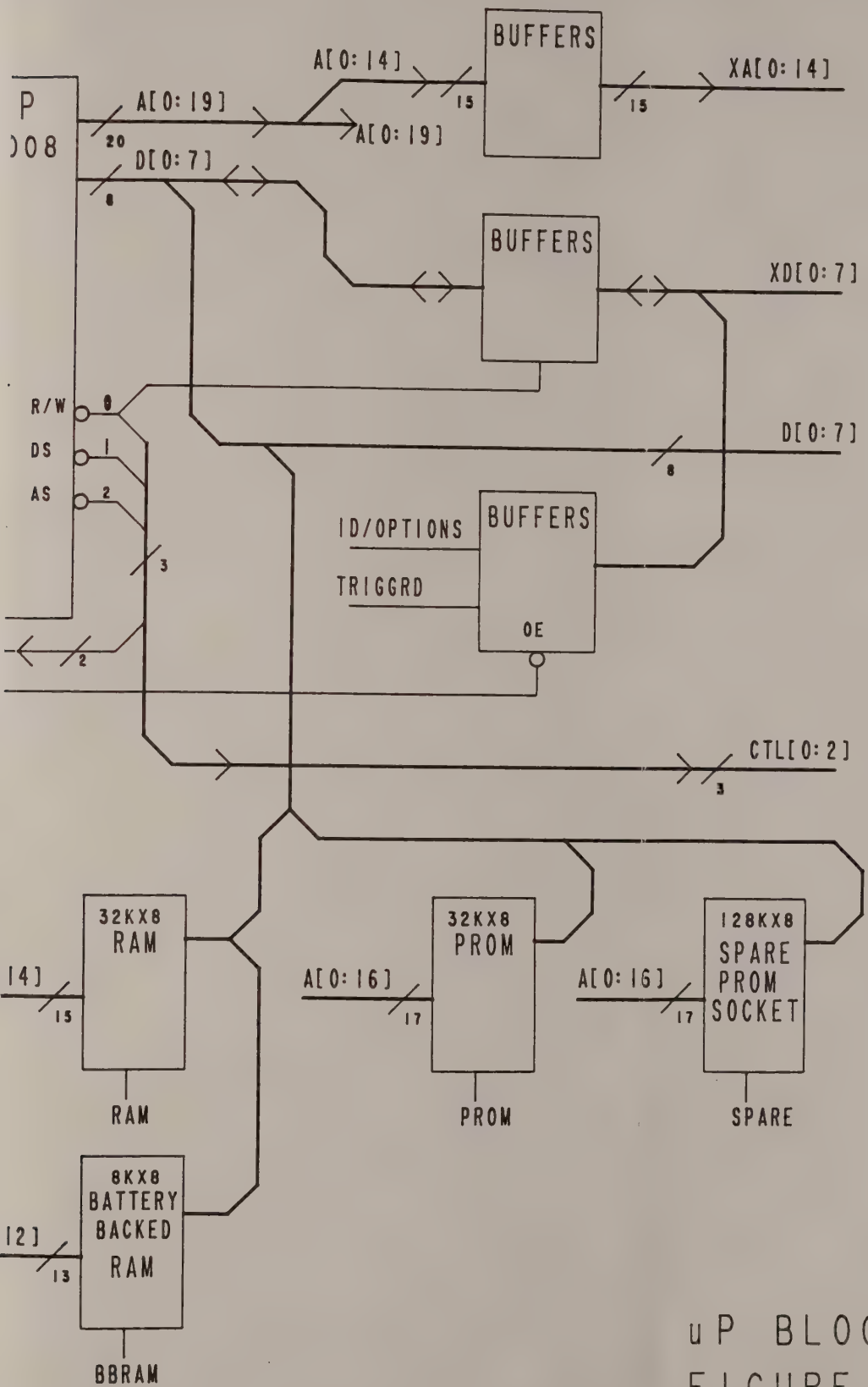
BLOCK DIAGRAM
9210MAIN SH 1 of 2
FIGURE 4-2



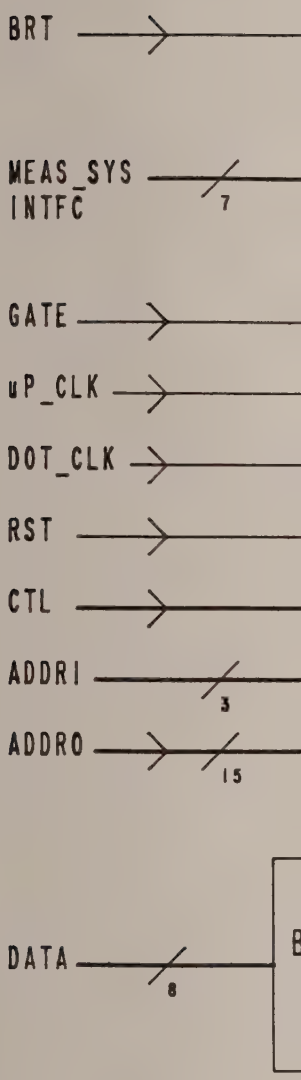
BLOCK DIAGRAM
9210MAIN SH 2 of 2
FIGURE 4-2 (CON'T)

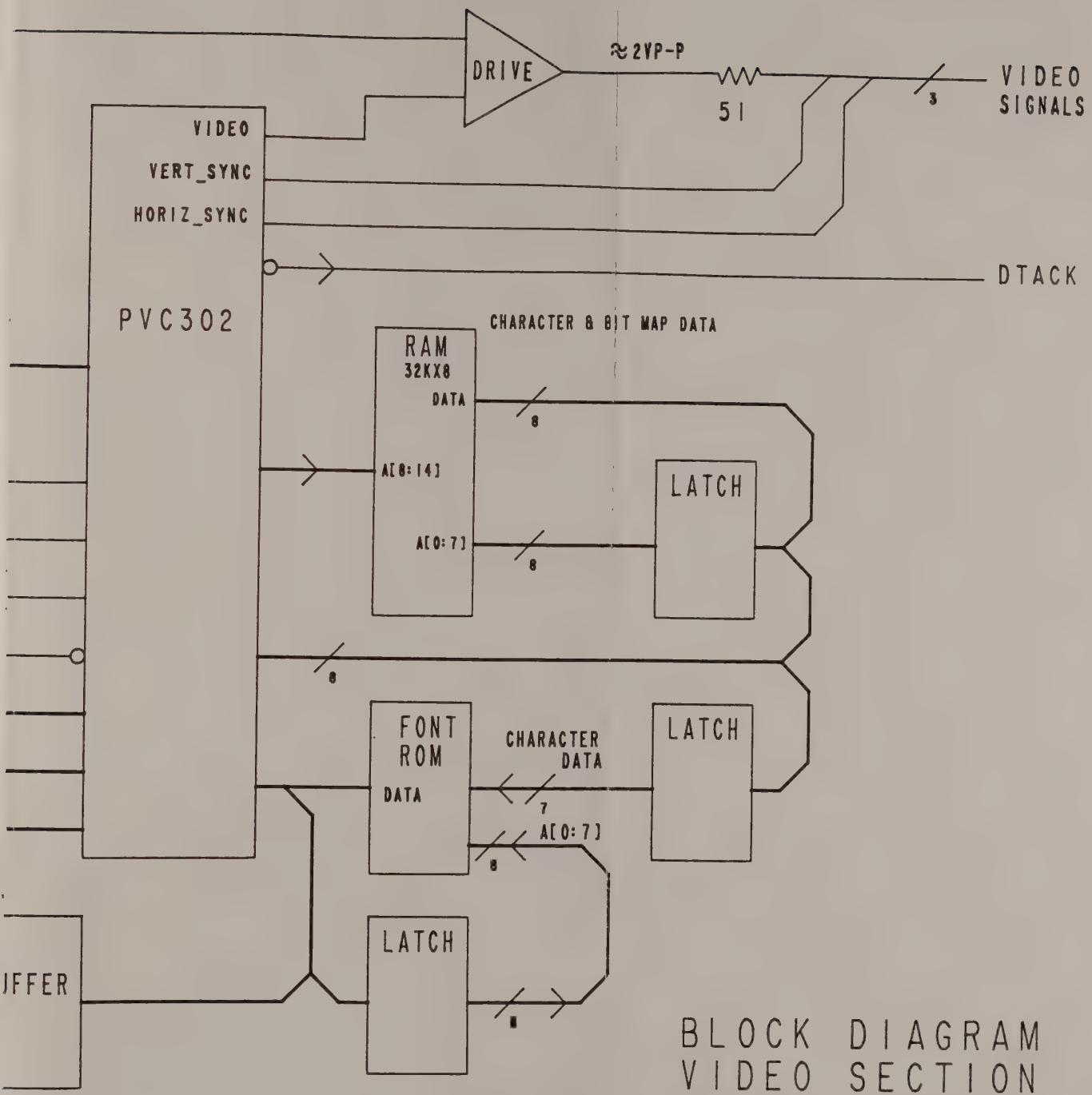

PI_CTL
TO SH.(1)
CH_A_PULSE*
CH_A_PULSE
MEAS SYS
TIMING IN
SH.(1)
-5VREF
DATA
CHANNEL_A
DELAY/WIDTH
SCHEM SH. 7
TRIG
TRIGN
WID_OUT
WID_OUT*
JA1
JA2
DLY_SLO_CNTR
WID_SLO_CNTR
CHIPSEL
CHG_STB
ADDR
RST
TDIN
FCAL
BUS
FCAL_BUS
MEAS SYS
TIMING IN
SH.(1)
TRIG_ERR_WID
TRIG_ERR_DLY
TDOUT
TRIGERR*
(IRQ[5])
CHA_TD
DTACK
CH_B_PULSE*
CH_B_PULSE
MEAS SYS
TIMING IN
SH.(1)
-5VREF
DATA
CHANNEL_B
DELAY/WIDTH
SCHEM SH. 8
TRIG
TRIGN
WID_OUT
WID_OUT*
JB1
JB2
DLY_SLO_CNTR
WID_SLO_CNTR
CHIPSEL
ACHG
ADDR
RST
TDIN
TRIG_CLK
FCAL
BUS
FCAL_BUS
TO SH.(1)
TRIG_ERR_WID
TRIG_ERR_DLY
TDOUT
≈ -2.9V
≈ 25uA
TDCHAIN
TO SH.(1)


XTAL
32mHZ
DIVDER
÷2 ÷4 ÷8
16MHZ
8MHZ
4MHZ
DOT_CLK
16MHZ
UP_CLK
CLK
XA[0:6]
J12
SUPERVISOR CKT.
RESET
DTACK*
IRQ
XA[1:5]
5
68901
8
XD[0:7]
IRQ
4mHZ
DTACK
R/W
DS
XA[0:6]
7
INTERRUPTS
CS
PAL
BBRAM
RAM
PROM
SPARE
A[12:19]
8
3:8 LINE DECODE
A[12:14]
3
5
CHIPSELECTS

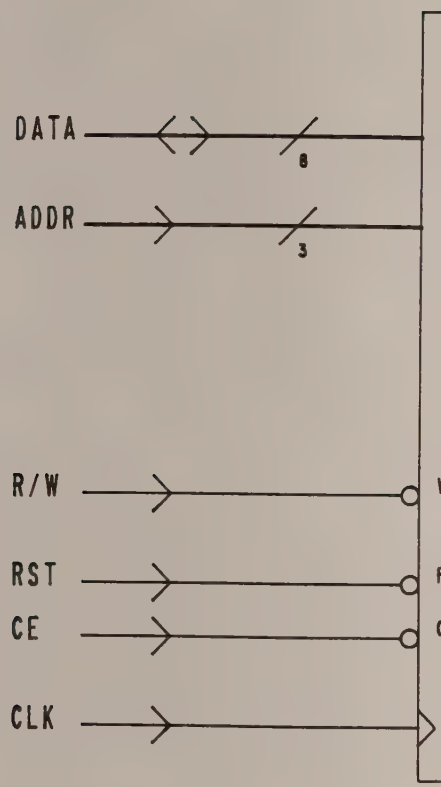


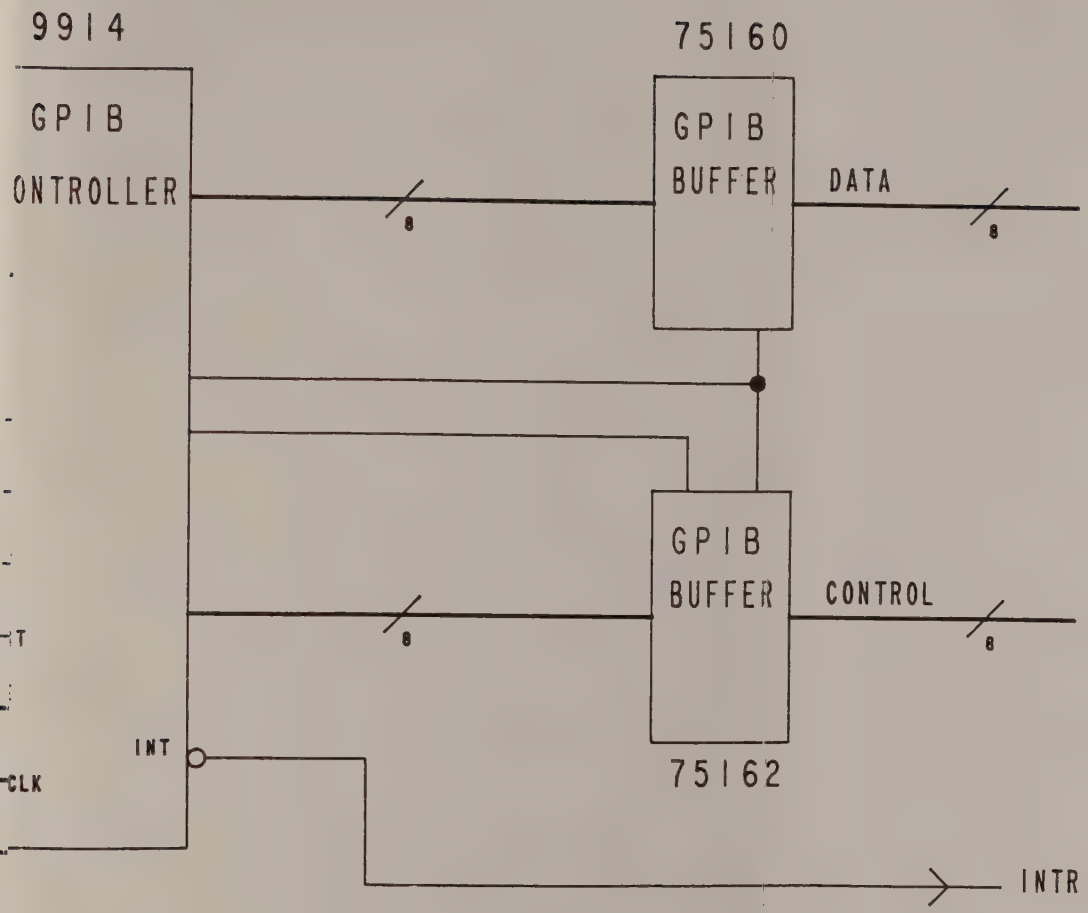
uP BLOCK DIAGRAM
FIGURE 4-2-1


BRT
MEAS_SYS
INTFC
7
GATE
uP_CLK
DOT_CLK
RST
CTL
ADDRI
3
ADDRO
15
DATA
8

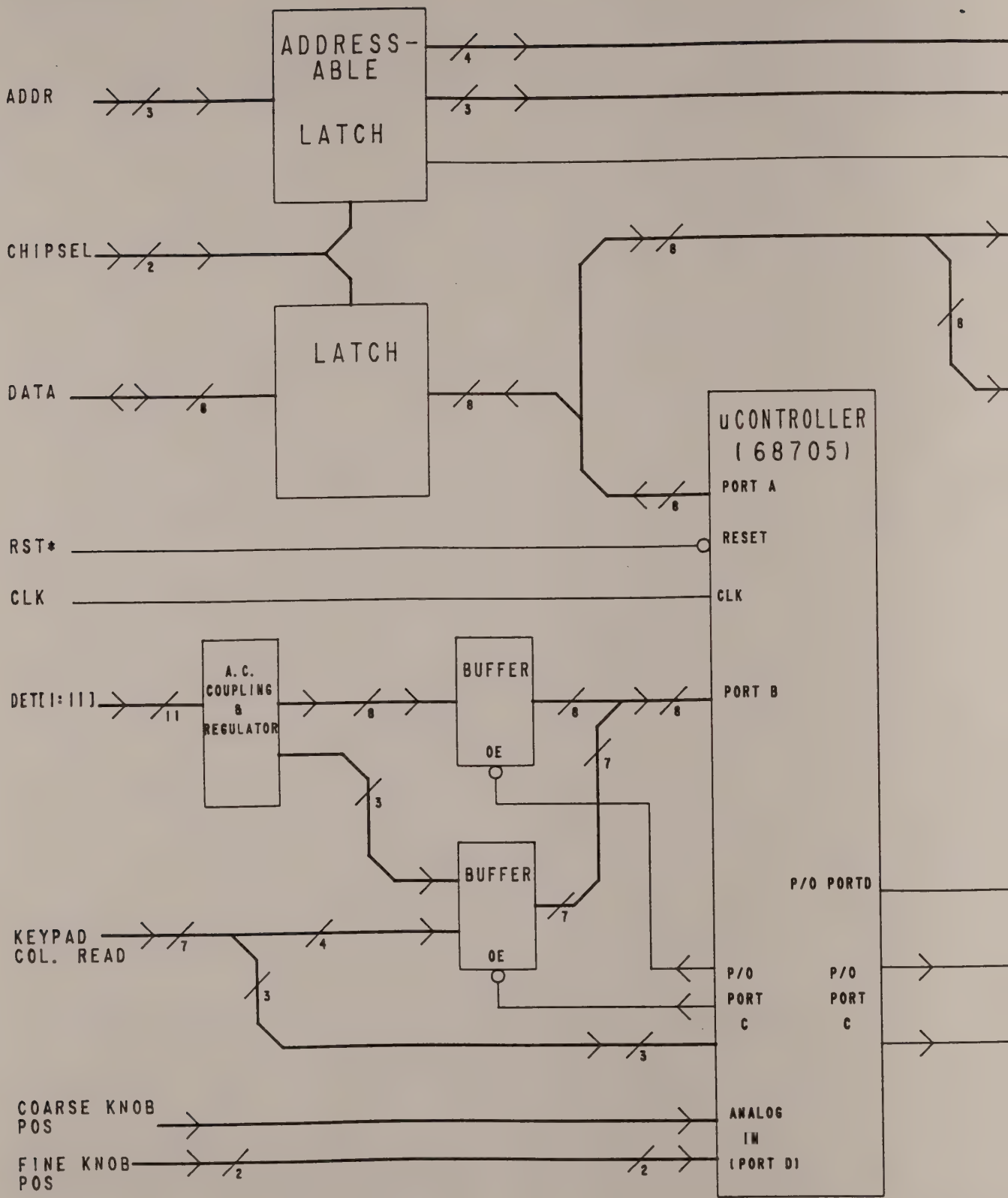


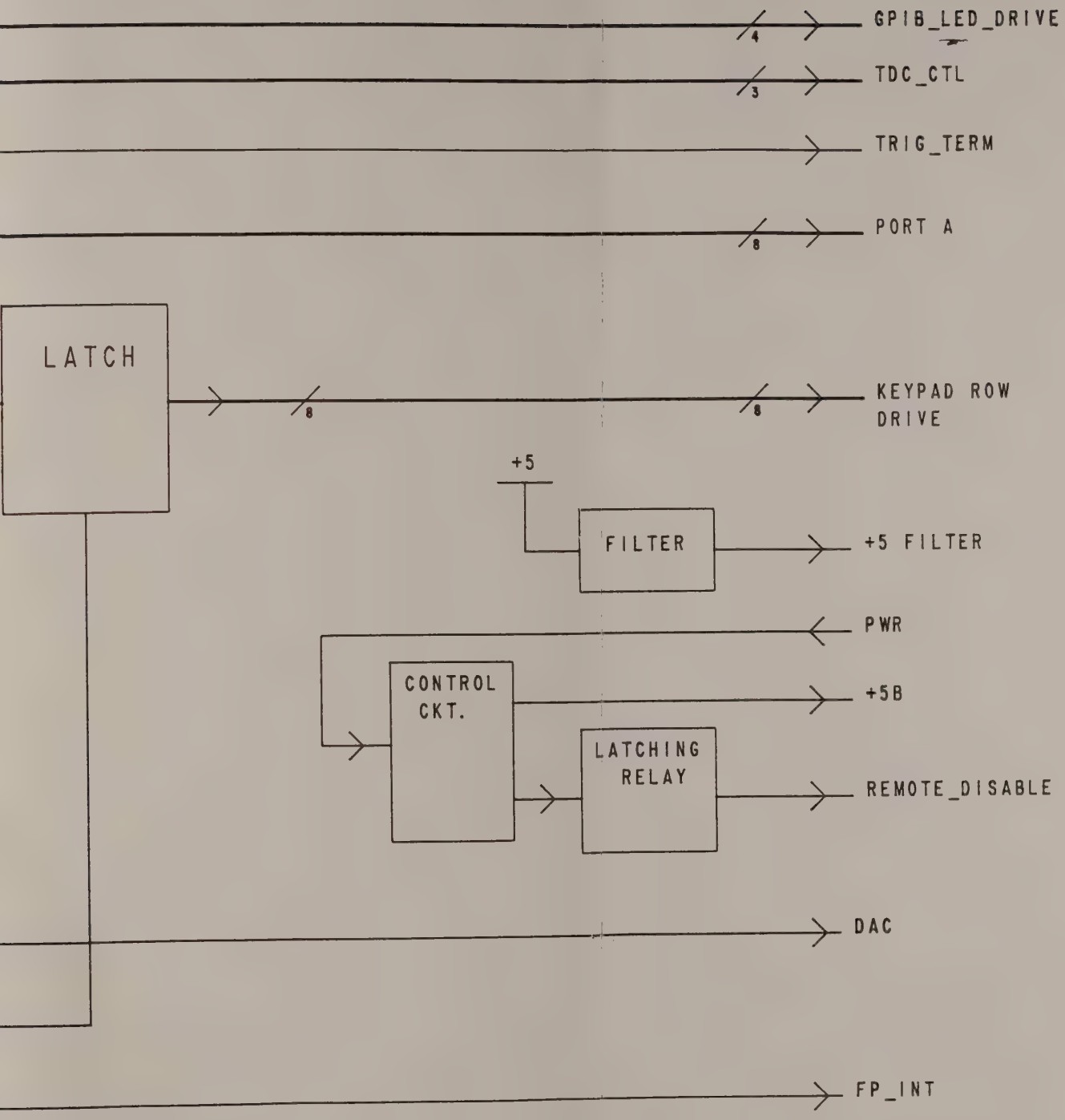
BLOCK DIAGRAM
VIDEO SECTION
FIGURE 4-2-2


DATA
8
ADDR
3
R/W
RST
CE
CLK

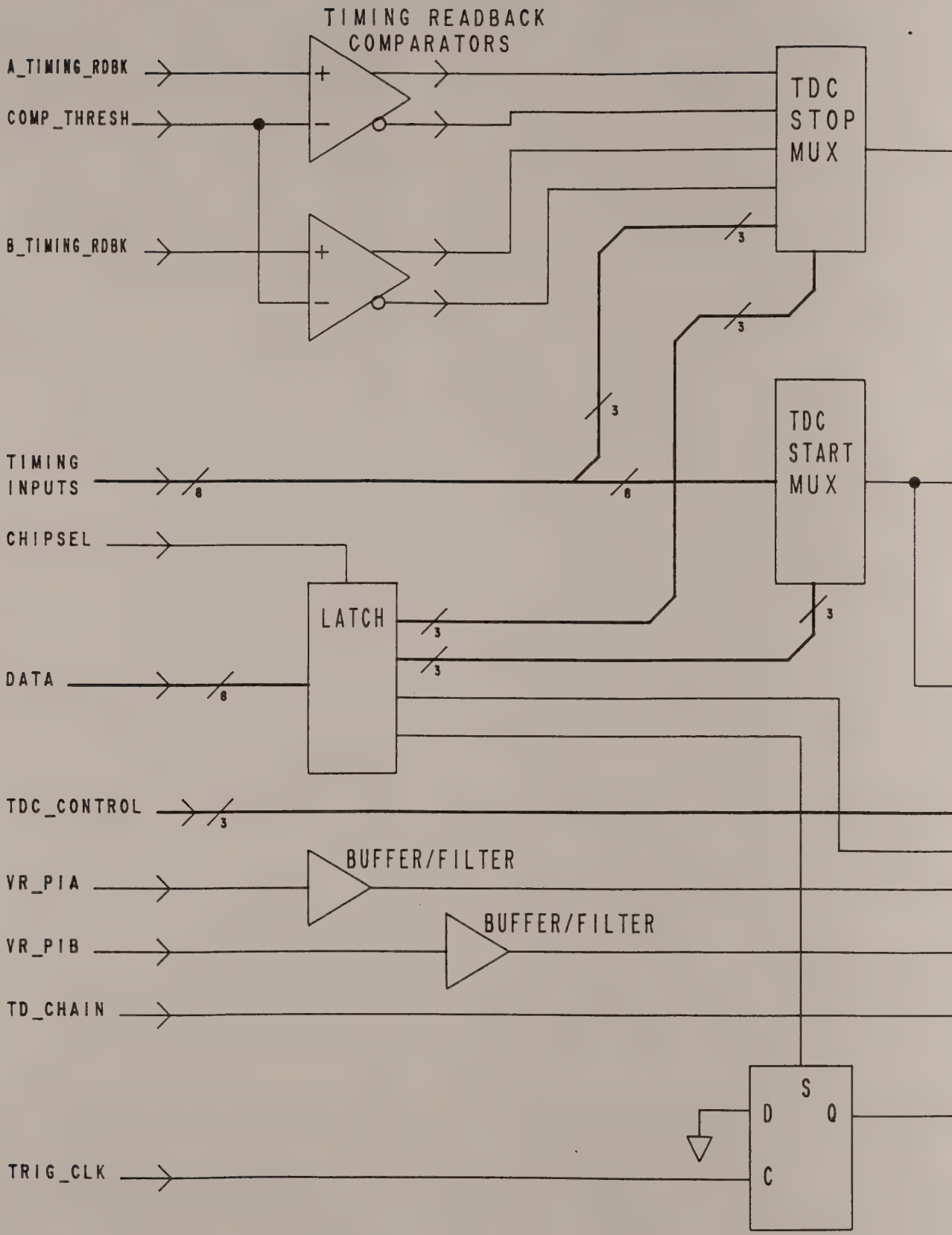


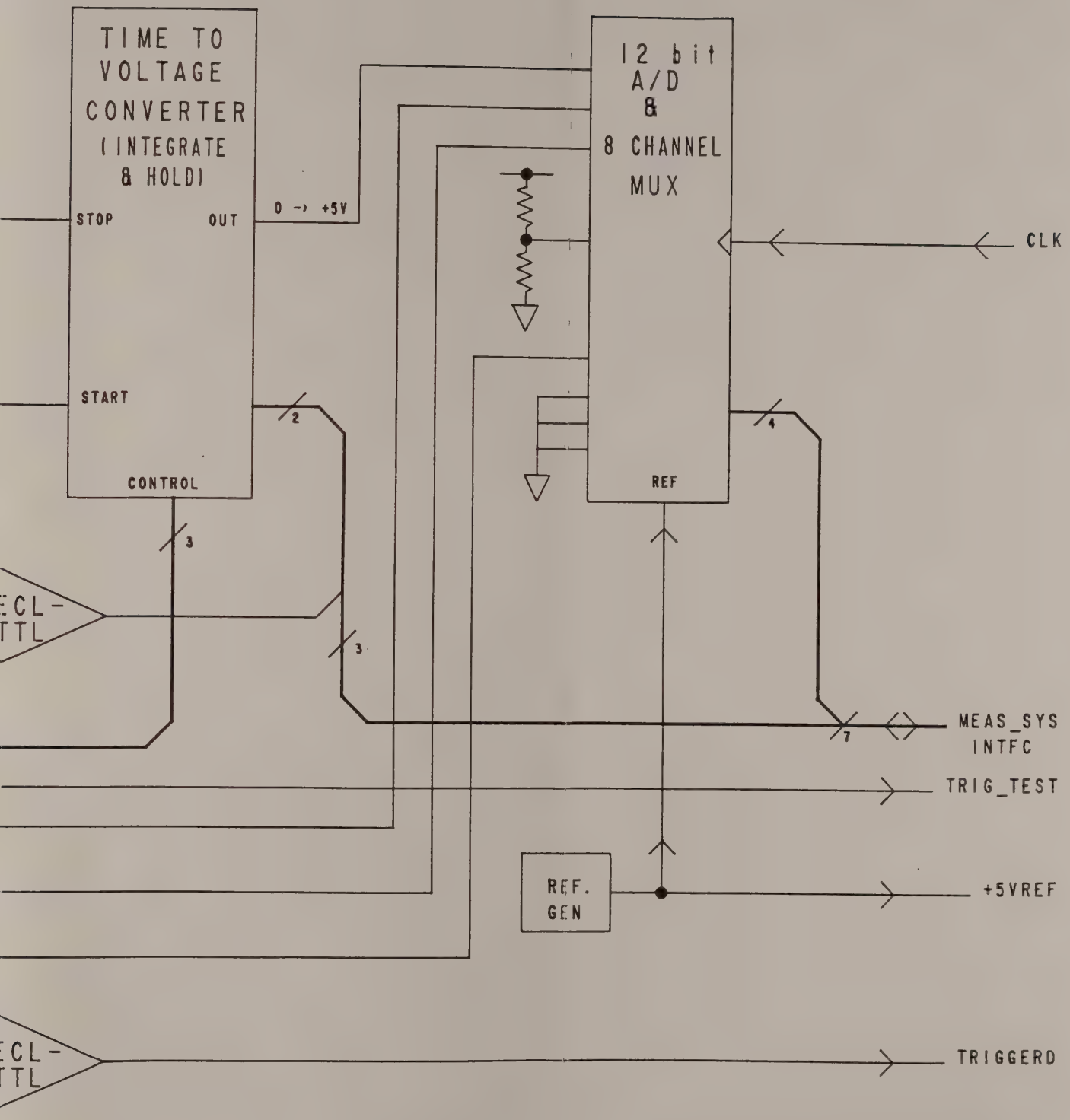
BLOCK DIAGRAM
GPIB
FIGURE 4-2-3


ADDRESS-
ABLE
LATCH
ADDR
3
4
3
CHIPSEL
2
LATCH
DATA
8
8
8
8
8
8
uCONTROLLER
(68705)
PORT A
RESET
RST*
CLK
CLK
A.C.
COUPLING
&
REGULATOR
DET[1:11]
11
8
BUFFER
OE
8
8
8
PORT B
7
3
BUFFER
OE
7
P/O PORTD
KEYPAD
COL. READ
7
4
3
P/O
PORT
C
P/O
PORT
C
3
COARSE KNOB
POS
FINE KNOB
POS
2
2
ANALOG
IN
(PORT D)

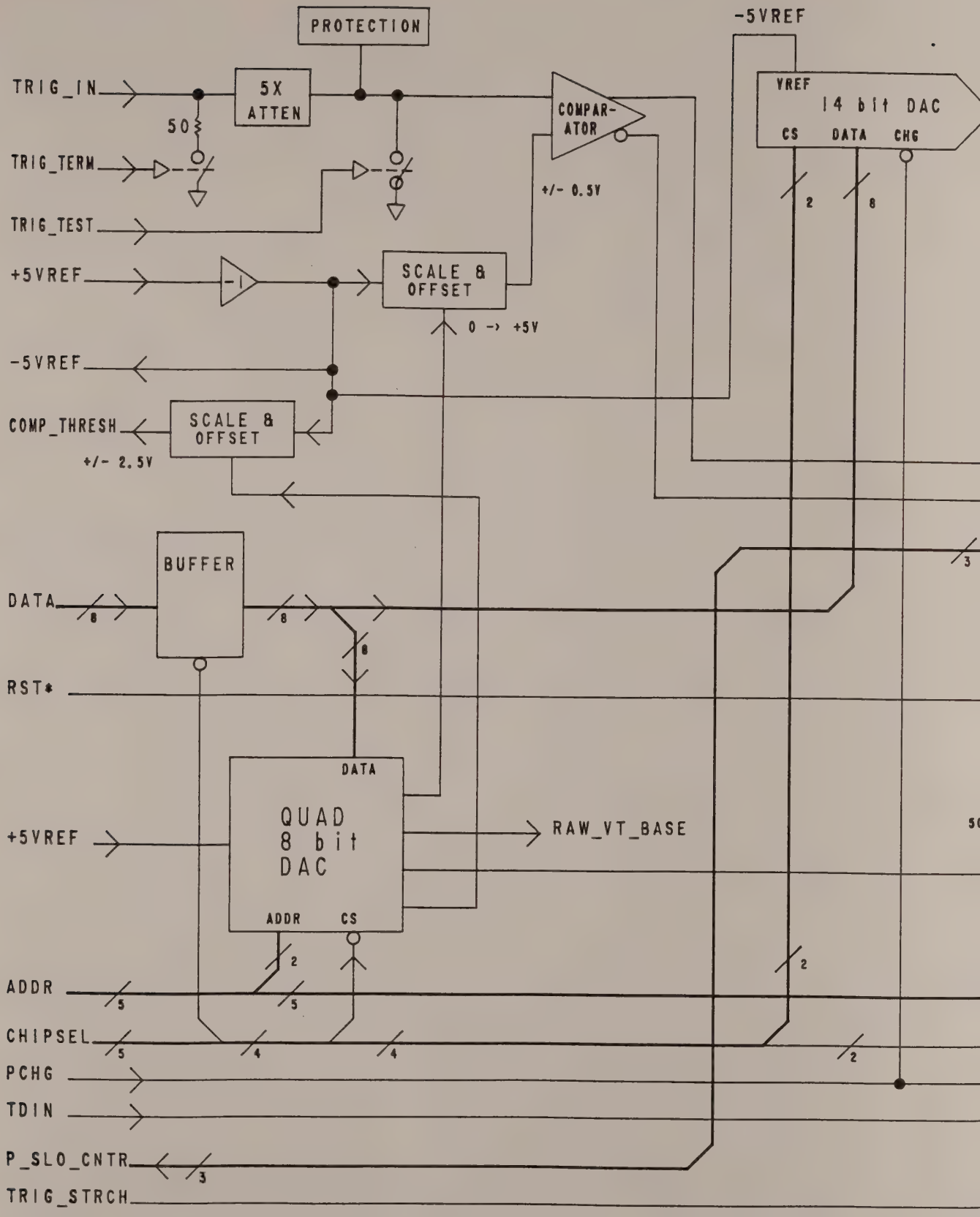


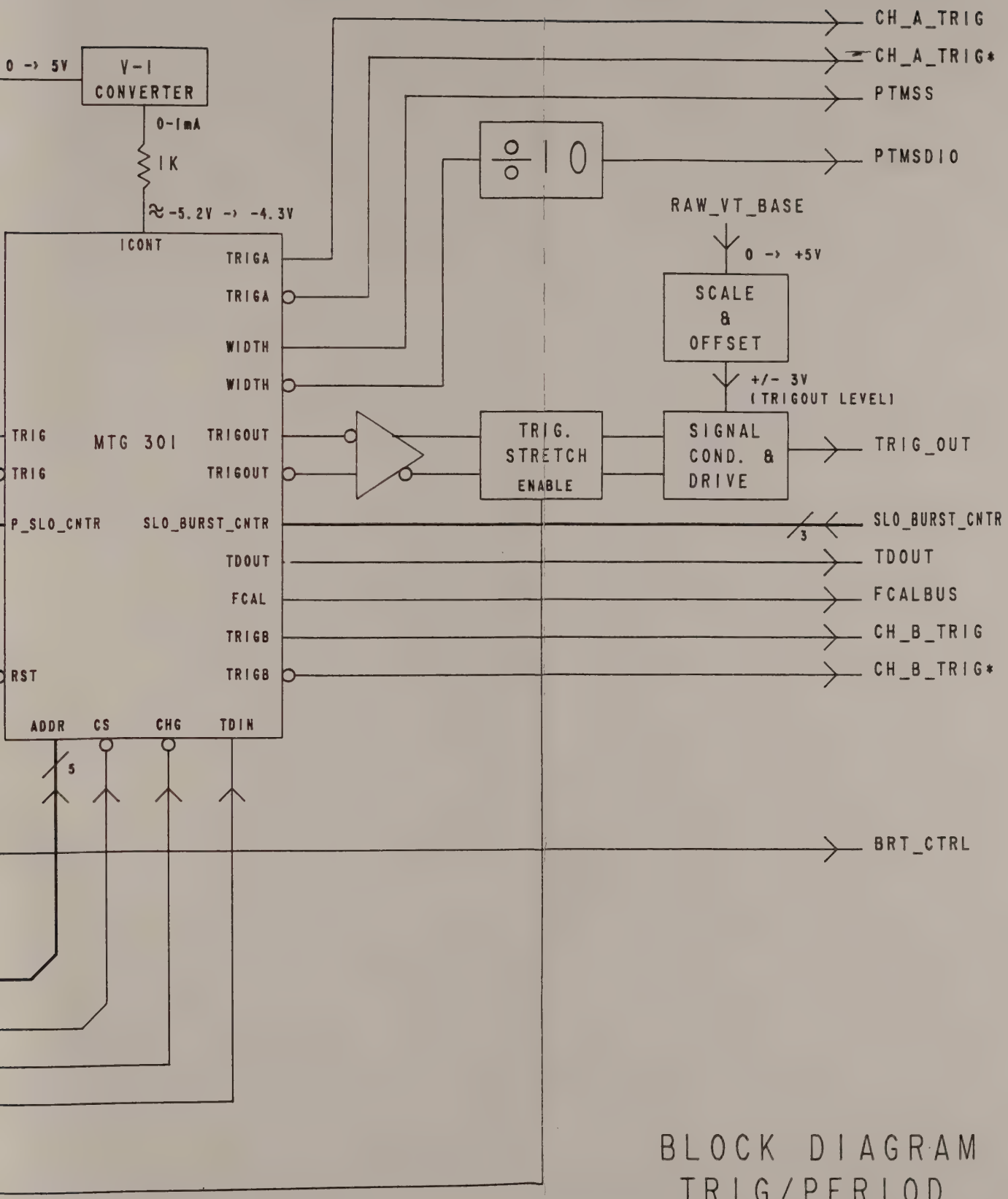
BLOCK DIAGRAM
FRONT PANEL INTERFACE
(9210)
FIGURE 4-2-4


TIMING READBACK
COMPARATORS
A_TIMING_RDBK
COMP_THRESH
B_TIMING_RDBK
+
−
+
−
TDC
STOP
MUX
TDC
START
MUX
TIMING
INPUTS
CHIPSEL
LATCH
DATA
TDC_CONTROL
BUFFER/FILTER
VR_PIA
BUFFER/FILTER
VR_PIB
TD_CHAIN
S
D
Q
C
TRIG_CLK
3
8

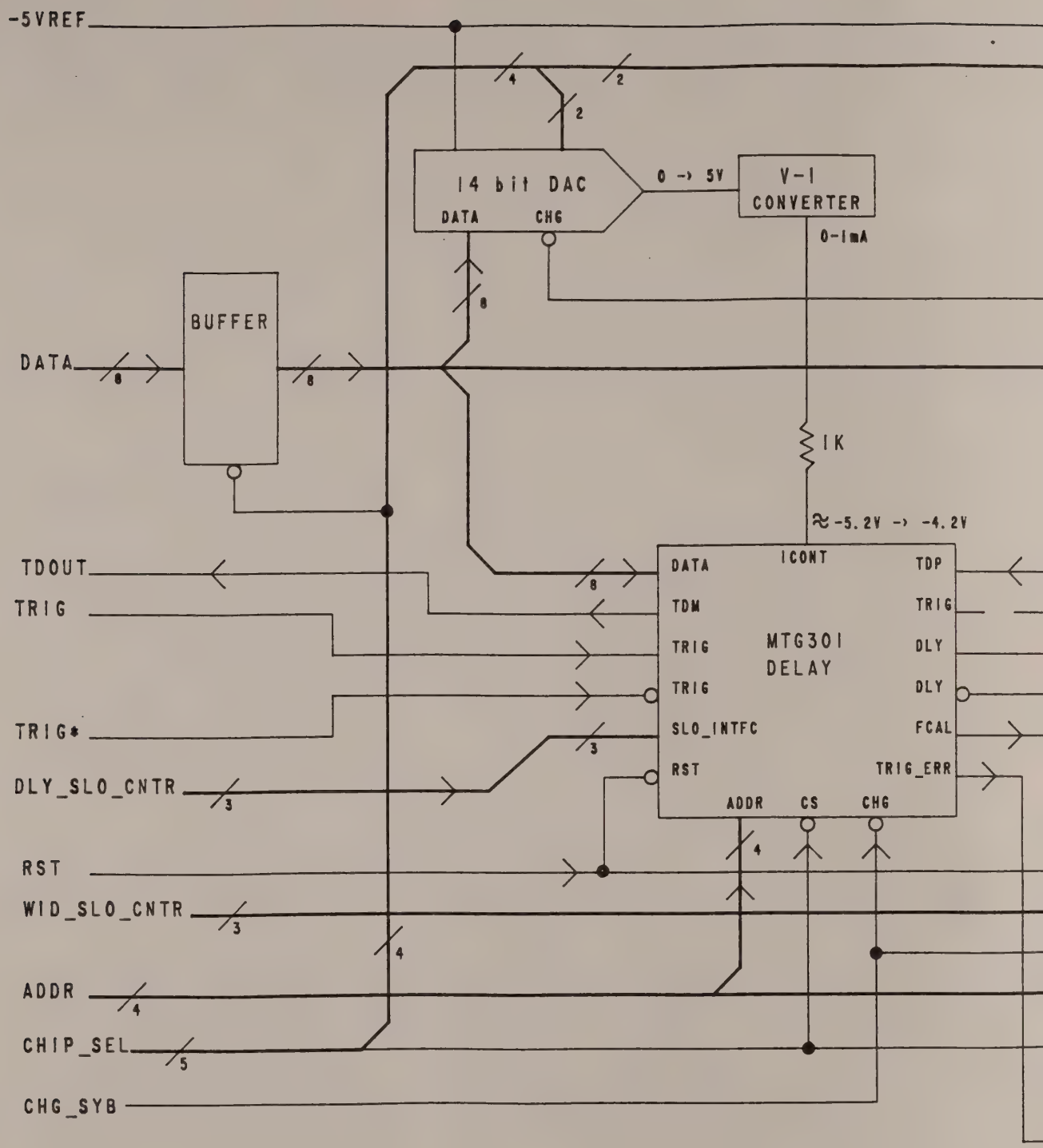


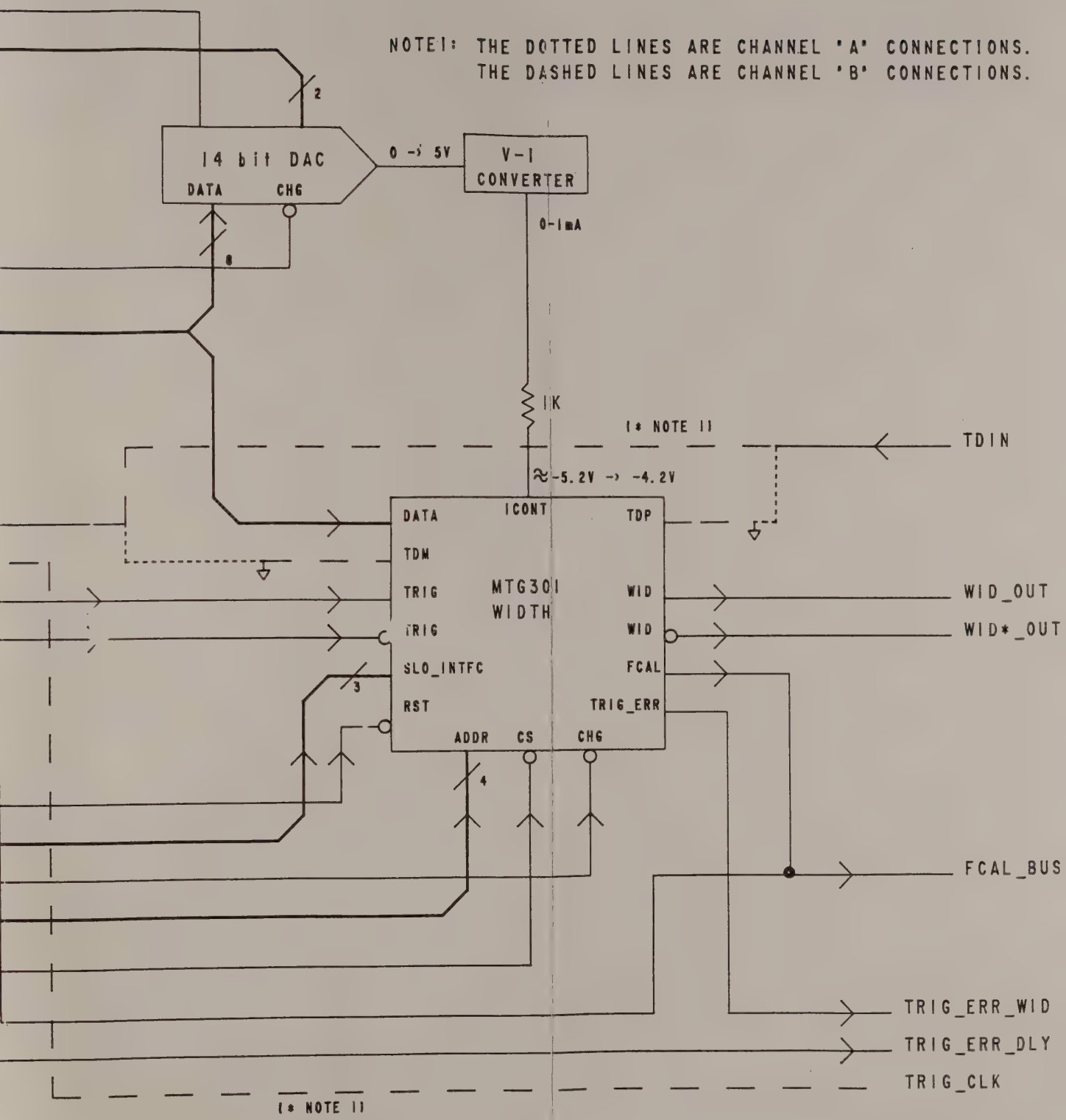
BLOCK DIAGRAM
MEASUREMENT SYSTEM
(9210)
FIGURE 4-2-5


PROTECTION
-5VREF
TRIG_IN
5X ATTEN
50
COMPAR- ATOR
VREF
14 bit DAC
CS
DATA
CHG
TRIG_TERM
TRIG_TEST
+/- 0.5V
+5VREF
-1
SCALE & OFFSET
0 -> +5V
-5VREF
COMP_THRESH
SCALE & OFFSET
+/- 2.5V
BUFFER
DATA
RST*
DATA
QUAD 8 bit DAC
+5VREF
RAW_VT_BASE
ADDR
CS
ADDR
CHIPSEL
PCHG
TDIN
P_SLO_CNTR
TRIG_STRCH



BLOCK DIAGRAM
TRIG/PERIOD
FIGURE 4-2-6


-5VREF
4
2
2
14 bit DAC
DATA
CHG
0 -> 5V
V-I
CONVERTER
0-1mA
8
BUFFER
DATA
8
8
1K
≈-5.2V -> -4.2V
TDOUT
TRIG
TRIG*
DLY_SLO_CNTR
3
RST
WID_SLO_CNTR
3
4
ADDR
4
CHIP_SEL
5
CHG_SYB
8
3
4
DATA
ICONT
TDP
TDM
TRIG
TRIG
MTG301
DELAY
DLY
TRIG
DLY
SLO_INTFC
FCAL
RST
TRIG_ERR
ADDR
CS
CHG



BLOCK DIAGRAM
DELAY/WIDTH
FIGURE 4-2-7

DISASSEMBLY

5.0 Introduction

This section includes the instrument disassembly and replacement procedures.

WARNING ***Disassembly described in this section is performed with power removed from the instrument. Do not remove or replace any of the circuit board assemblies without first verifying that power has been removed from the instrument.***

Anti-static protection measures should be taken prior to the handling of any printed circuit boards.

5.1 Power Supply

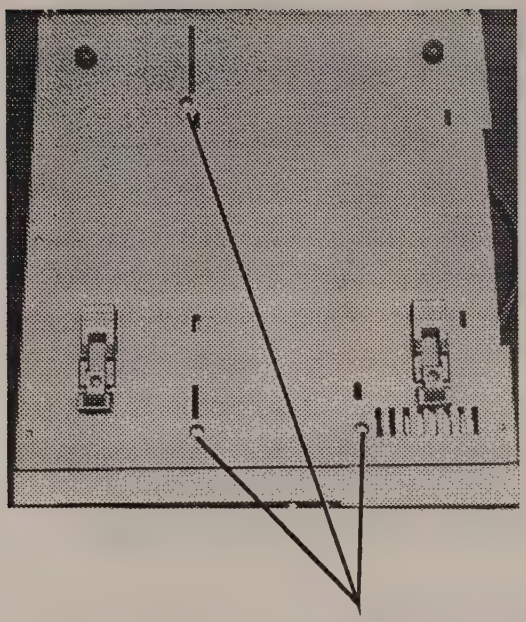
POWER SUPPLY REMOVAL

1. Disconnect power cable from the instrument.
2. Remove the three screws from the bottom cover as shown in F5.2.2
3. Remove the two screws from the rear panel as shown in F5.2.3
4. Carefully remove the top cover from the unit by lifting the back portion first, approximately two inches, slide the cover slightly to the rear, then gently lift the cover up.
5. Remove the screw which attaches the power supply to the rear panel as shown in F5.2.5.
6. If applicable, disconnect the grounding jumper from power supply as shown in F5.2.6.
7. Carefully raise the front end of the power supply, lift the supply clear of the instrument, then disconnect the cable harness from P3 of the mainboard.

NOTE ***Depress locking tab when removing P3***

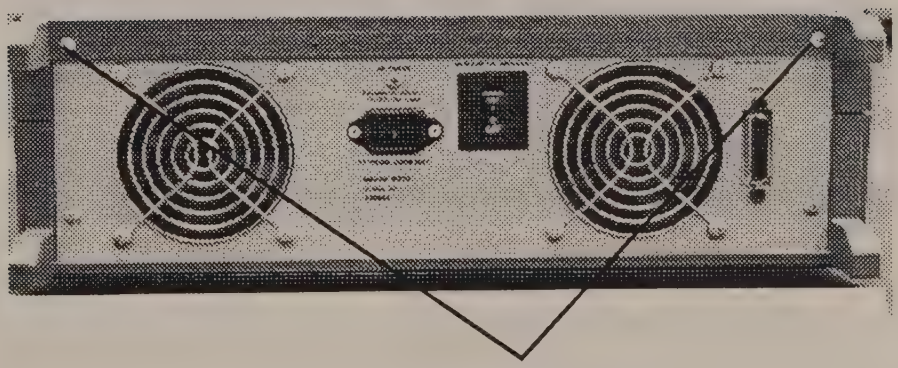
5.2 POWER SUPPLY REPLACEMENT

1. Reverse the removal procedure to install the power supply.



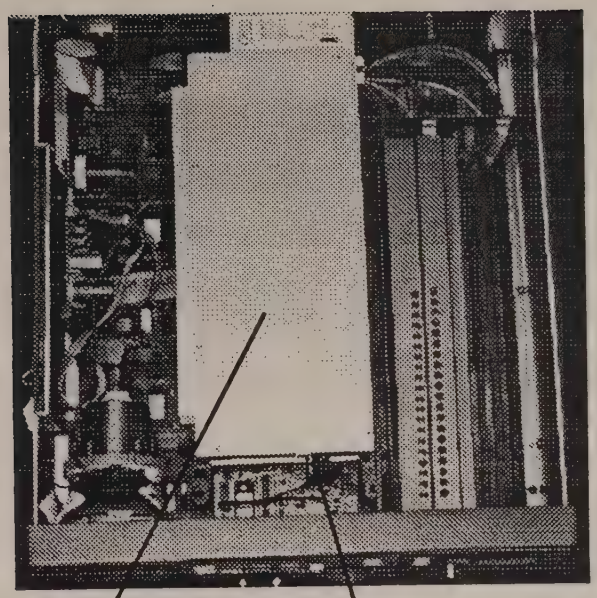
(3) Screw Philips 8-32 x 3.25"
560-832-052

F5.2.2 Bottom View

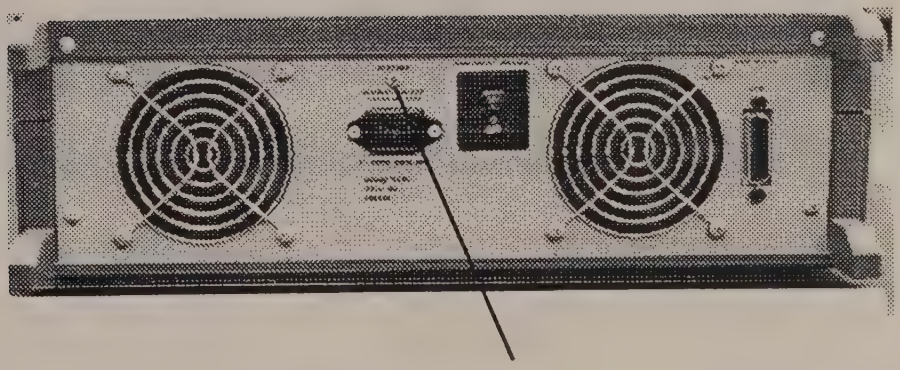


(2) Screw philips 8-32 x 1/2
560-832-008

F5.2.3 Rear View



F5.2.6 Top View



(1) Screw philips 8-32 x 1/2
560-832-008

F5.2.5 Rear View

5.3 Fan

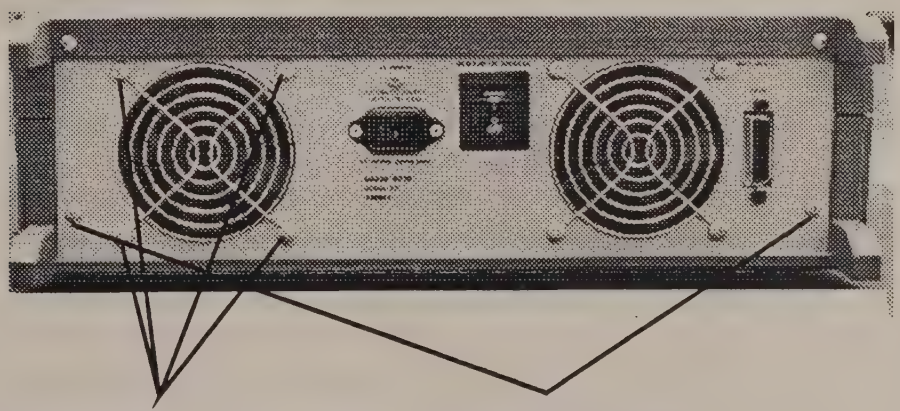
FAN REMOVAL

1. Disconnect power cable from the instrument.
2. Perform the Power Supply Removal procedure (Sect. 5.2).
3. Remove the two screws that attach the rear panel to the instrument as shown in F5.3.3.
4. Disconnect the fan power cables P6 and P7, and the GPIB cable J17 from the mainboard.
5. Remove the Rear Panel from the instrument.
6. Remove the four screws holding the Fan Guard and Fan in place as shown in F5.3.3

NOTE *When removing the Fan Guard and Fan, use a Torx driver T20.*

FAN REPLACEMENT

1. Reverse the removal procedure to install the fan(s).



(4) Screw Torx 10-10 x 13/16
561-010-113

(2) Screw Philips 8-32 x 3.25"
560-832-052

F5.3.3 Rear View

5.4 Backplane Assembly

BACKPLANE ASSEMBLY REMOVAL

1. Disconnect power cable from the instrument.
2. Perform the Power Supply Removal procedure (Sect. 5.2).
3. Perform the Fan Removal procedure to step 5 (Sect. 5.3)
4. Disconnect signal cables J8 - J10, J14, and J15, from the mainboard.
5. Carefully lift the Backplane out of the instrument.

NOTE ***To remove the signal cables from the backplane use EJECTOR TOOL #594233 with EJECTORTOOL INSERT #433222. These can be obtained from: Erni Components, 520 Southlake Blvd., Richmond, Virginia USA 23236***

BACKPLANE ASSEMBLY REPLACEMENT

1. Reverse the removal procedure to install the Backplane Assembly. See that the signal cables are properly routed through the notch in the instruments center support wall. See F5.5.7 for Backplane to Motherboard cable connections.

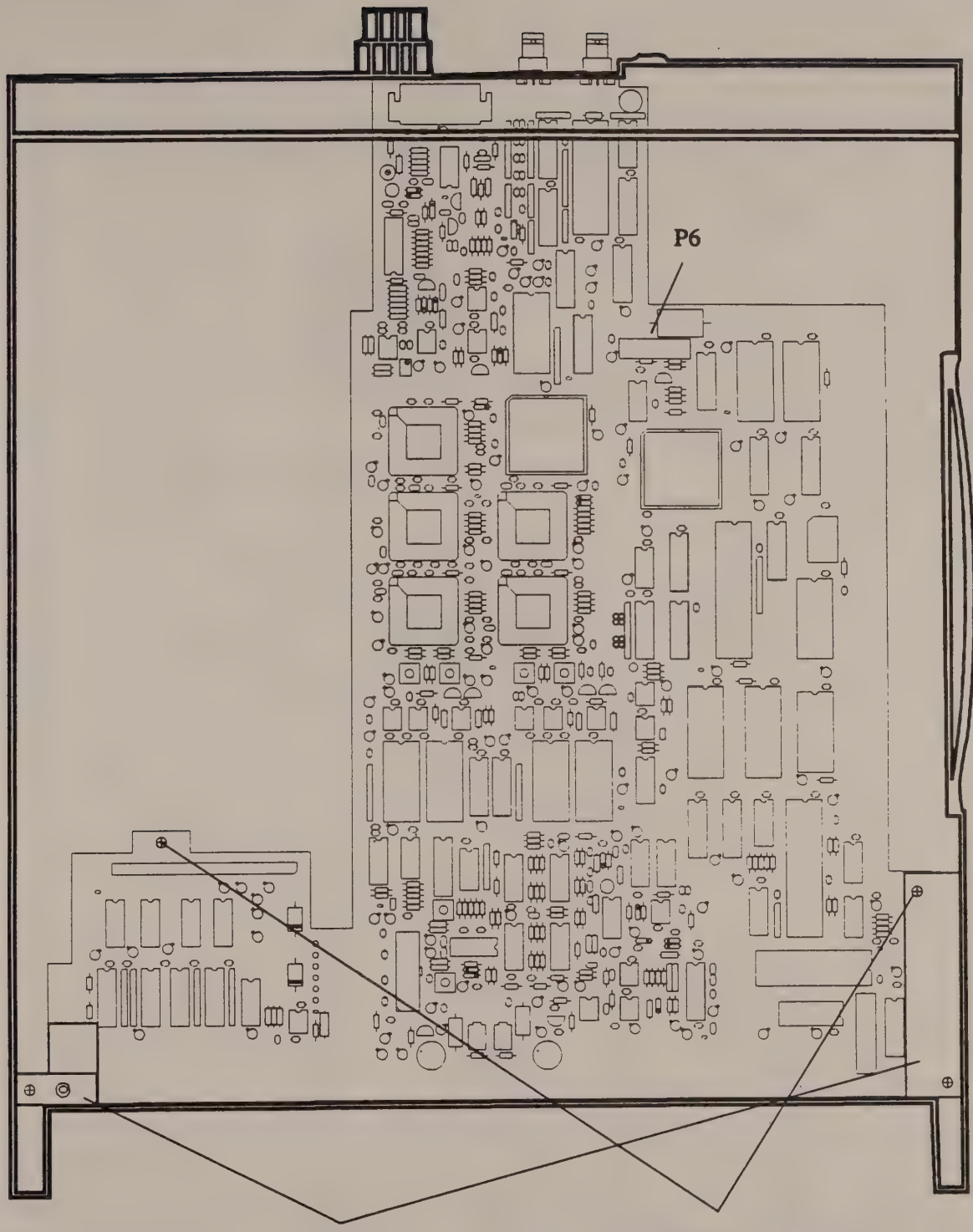
5.5 Mainboard

MAINBOARD REMOVAL

1. Disconnect power cable from the instrument.
2. Perform the Power Supply Removal procedure (Sect. 5.2).
3. Perform the Fan Removal procedure to step 5 (Sect. 5.3).
4. Perform the Backplane Assembly Removal procedure (Sect. 5.4).
5. Disconnect the Video Signal cable from P6 on the mainboard.
6. If applicable, remove the two grounding brackets from the rear left and right of the mainboard.
7. Remove the two screws that attach the mainboard to the instrument's bottom housing as shown in F5.5.8.
8. Carefully slide the mainboard out of the rear of the instrument.

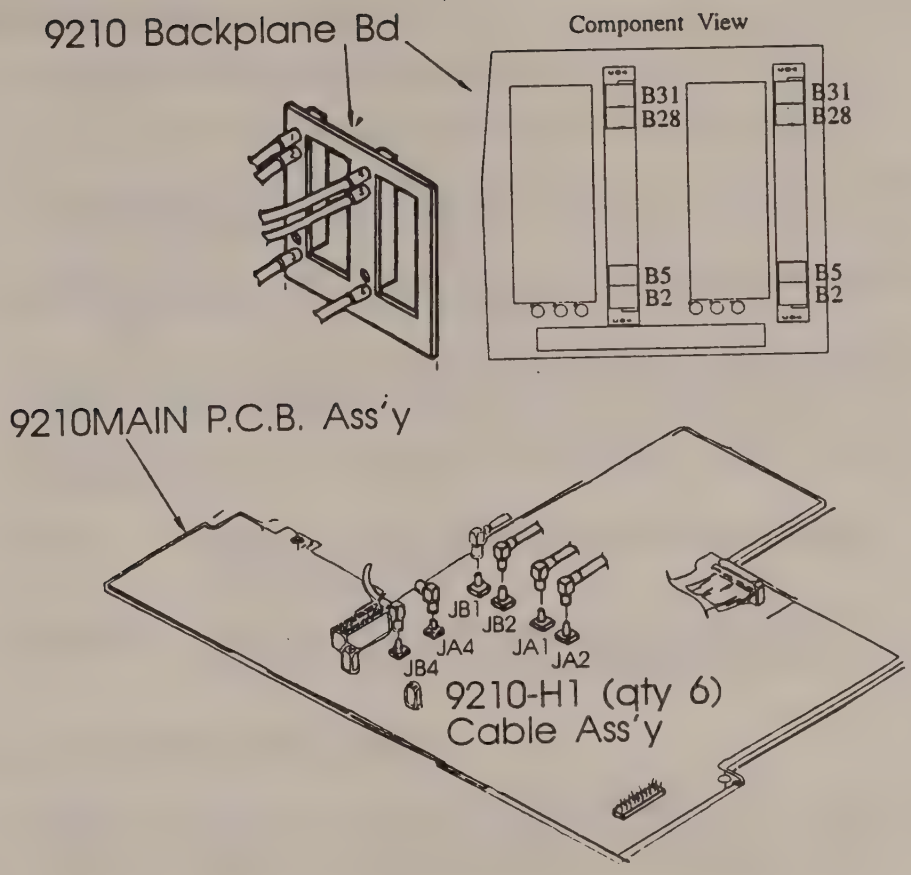
MAINBOARD REPLACEMENT

1. Reverse the removal procedure to install the mainboard. See F5.5.7 for Backplane to Mainboard cable connections.



Grounding Brackets	(2) #8 x 3/8" Machine screw (phil pan hd) 560-832-006

F5.5.7 Mainboard Bottom Housing



CABLE ROUTING

	Backplane		to 9210main board	
			Rev B	Rev A
Channel A	B31	--	JA1	(J10)
	B28	--	JA2	(J11)
	B5	--	Not Used	
	B2	--	JA4	(J14)
Channel B	B31	--	JB1	(J8)
	B28	--	JB2	(J9)
	B5	--	Not Used	
	B2	--	JB4	(J15)

F5.5.8 9210 Mainboard to Backplane Cables

5.6 CRT And Video Assembly

CRT AND VIDEO ASSEMBLY REMOVAL

1. Disconnect power cable from the instrument.

2. Perform the Power Supply Removal procedure to step 4 (Sect. 5.2).

3. Remove the four screws which attach the instrument's Front Bezel Assembly to the bottom housing as shown in F5.6.3.

4. Carefully lift out the Video PC board and disconnect the Video Signal cable. Rest the Video PC board to the side of the instrument.

5. Remove the Front Bezel Assembly from the instrument. A gentle rocking motion from left to right will assist in dislodging the assembly from the instrument.

6. Remove the four screws that attach the CRT to the Front Bezel Assembly as shown in F5.6.6.

NOTE ***When removing the CRT from the Front Bezel Assembly, use a Torx driver T20.***

WARNING ***Observe caution, High Voltage is present on the CRT and VIDEO ASSEMBLY while instrument is powered on.***

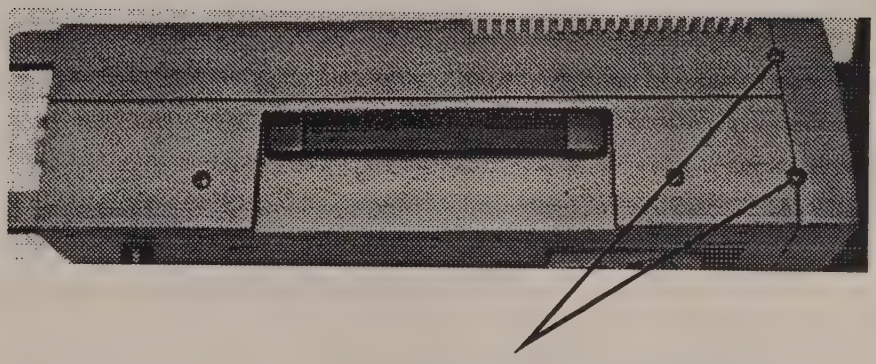
CRT AND VIDEO ASSEMBLY REPLACEMENT

1. Install the four screws that attach the CRT to the Front Bezel Assembly. While installing the CRT, apply firm pressure towards the closest side of the bezel to assure proper display alignment. Remember to attach the ground cable.

CAUTION ***Placing the bezel assembly on a raised surface with a hole for the Front Panel Control Knob to pass through, is recommended when attaching the CRT to the Front Bezel Assembly. This will prevent any potential damage to the Control Knob assembly.***

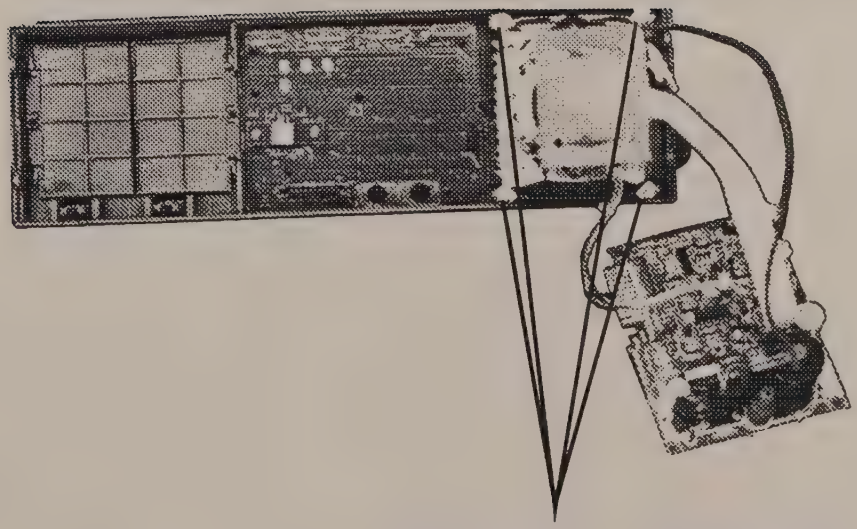
2. Reverse the removal procedure to install the CRT and Video Assembly.

CAUTION ***When reinstalling Front Bezel Assembly make sure the CRT shield doesn't get caught up on the edge of the 9210 Mainboard. Also, make sure the connection between the Front Panel PC board and the 9210 Mainboard are lined up and firmly connected together.***



(4) Machine screw #10 x 3/8"
555-502-006

F5.6.3 Side View (left)



(4) Screw, Torx 10 - 10 x 13/16"
Self-Tapping 560-832-008

F5.6.6 Front Panel Assembly

5.7 Front Panel PC Board And Soft Keys

FRONT PANEL PC BOARD AND SOFT KEYS REMOVAL

1. Disconnect power cable from the instrument.
2. Perform the CRT and Video Assembly removal procedure (Sect. 5.6).
3. Remove the cap from the Front Panel Knob Assembly as shown in F5.7.3.
4. Remove the screw and washer that attaches the inner control knob.
5. Loosen the outer knob retaining nut and remove the outer knob.
6. Remove the eight screws attaching the Front Panel PC Board to the Front Panel Assembly as shown in F5.7.6.
7. Remove the Front Panel soft key pad.

FRONT PANEL PC BOARD AND SOFT KEY REPLACEMENT

1. Reverse the removal procedure to install the Front Panel PC Board and Soft Keys.

NOTE ***Check all soft keys for clean action after securing the Front Panel PC Board into the front panel***

Do not overtighten the outer knob retaining nut. This will cause the outer and inner knobs to conflict preventing, proper operation.

Exercise caution when attaching the Front Panal Assembly to the instrument. Carefully observe the insertion of the Front Panel PC Board P3 into the Mainboard.

9210 MAINFRAME TROUBLESHOOTING

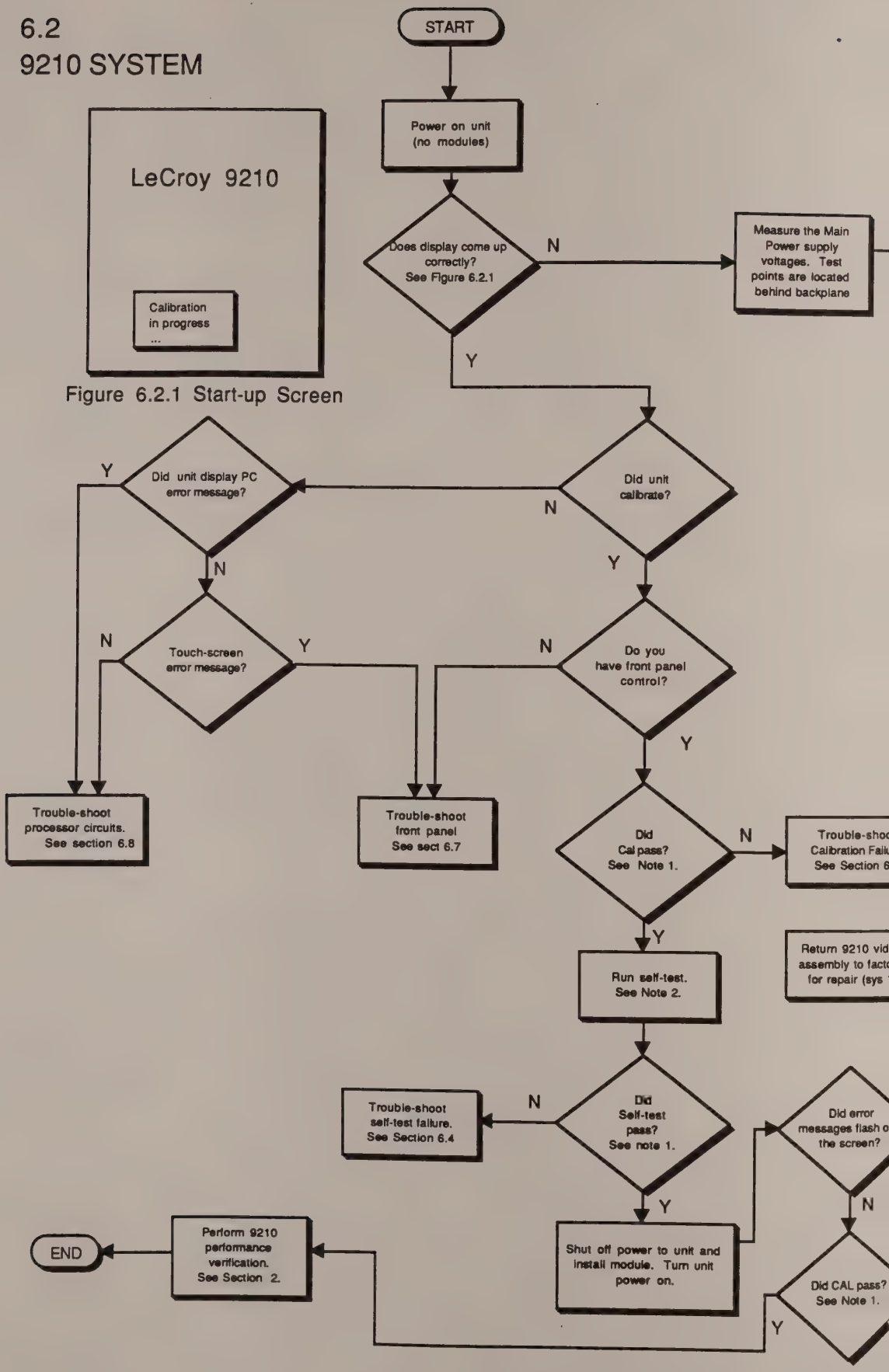
6.1 Introduction

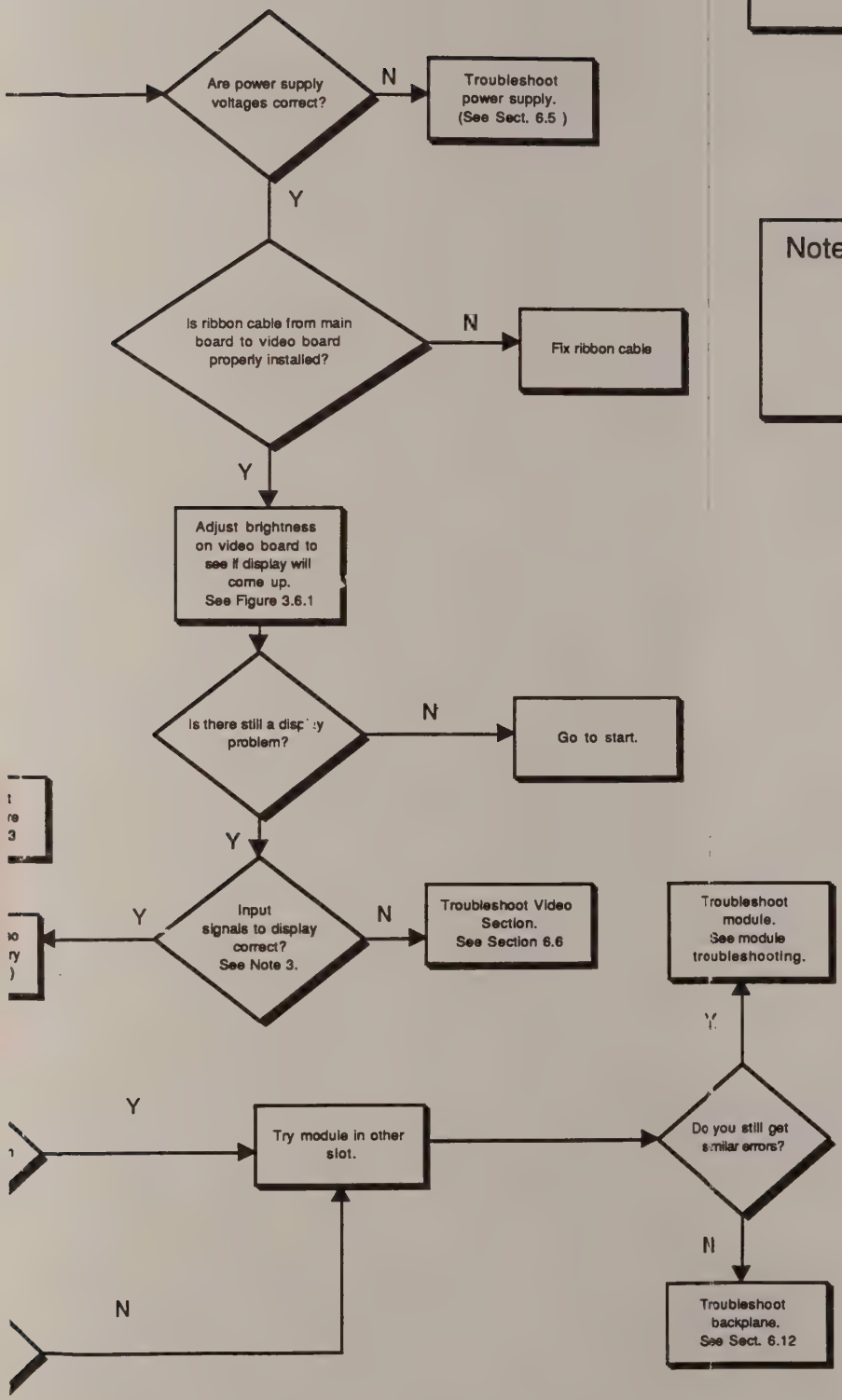
This section will guide service personnel in troubleshooting the 9210 Mainframe by the use of flow charts. The section is divided into 11 parts:

1. 9210 SYSTEM
2. CALIBRATION FAILURE
3. SELFTEST FAILURE
4. POWER SUPPLY
5. VIDEO
6. FRONT PANEL
7. PROCESSOR CIRCUIT
8. TRIGGER IN
9. TRIGGER OUT
10. GPIB
11. BACKPLANE

NOTE *When returning a part to the factory, please reference the malfunction code to customer service (where applicable).*

Figure 6.2.1 Start-up Screen



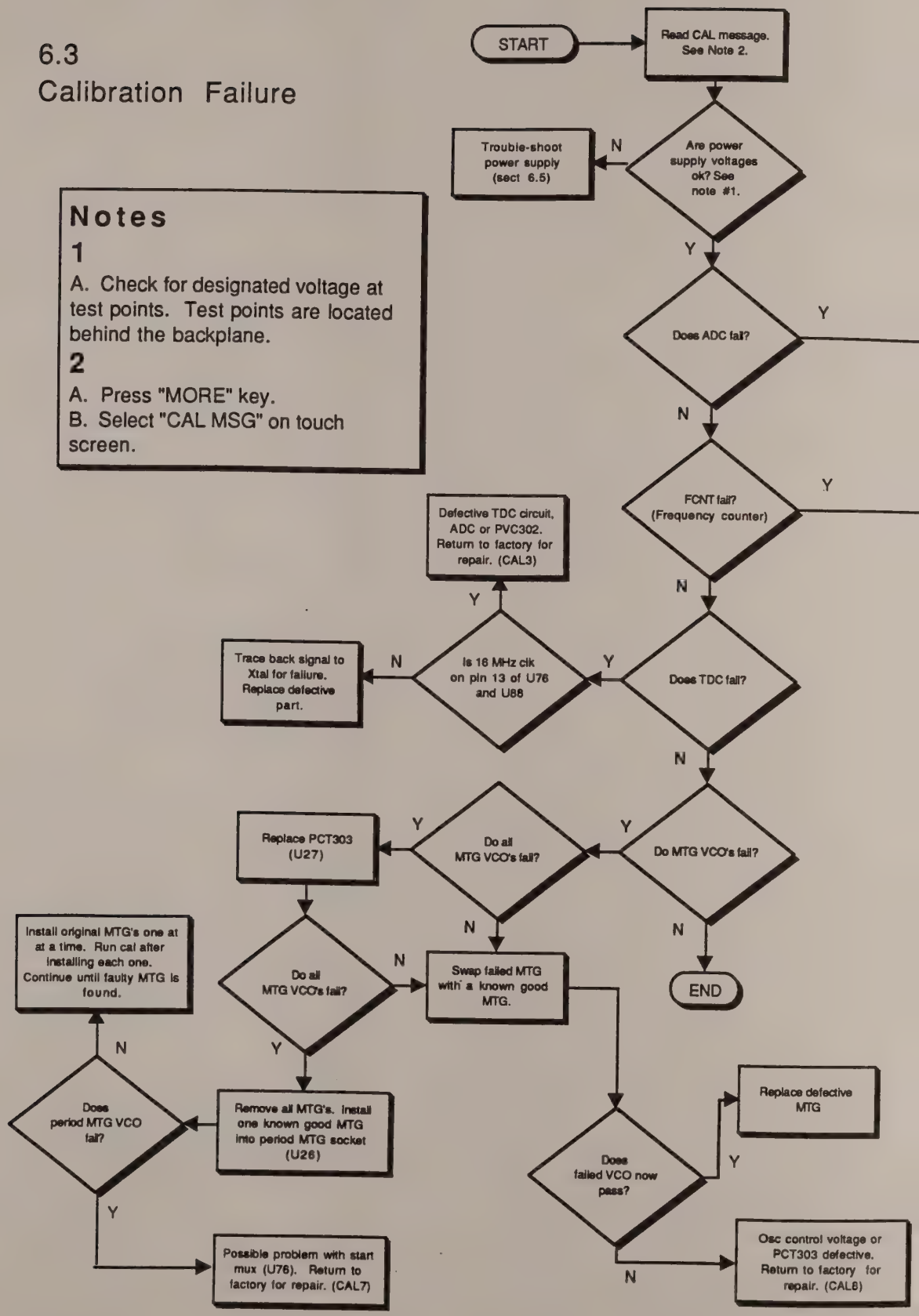


Note 1) A) Press the "More" button on front panel.
B) Select "Cal Msg" on touch screen.

Note 2) A) Press the "More" button on front panel.
B) Select "Selftest" on touch screen and execute.

Note 3) The input signals for the display are as follows:
Pixel Rate: 16.00 MHz (500 nS/point)
Horizontal Sync Rate: 21.98 KHz (45.5 uS)
Horizontal Sync Width: 4.5 uS
Vertical Sync Rate: 57.09 Hz (17.52 mS)
Vertical Sync Width: 682.5 uS

6.3
Calibration Failure



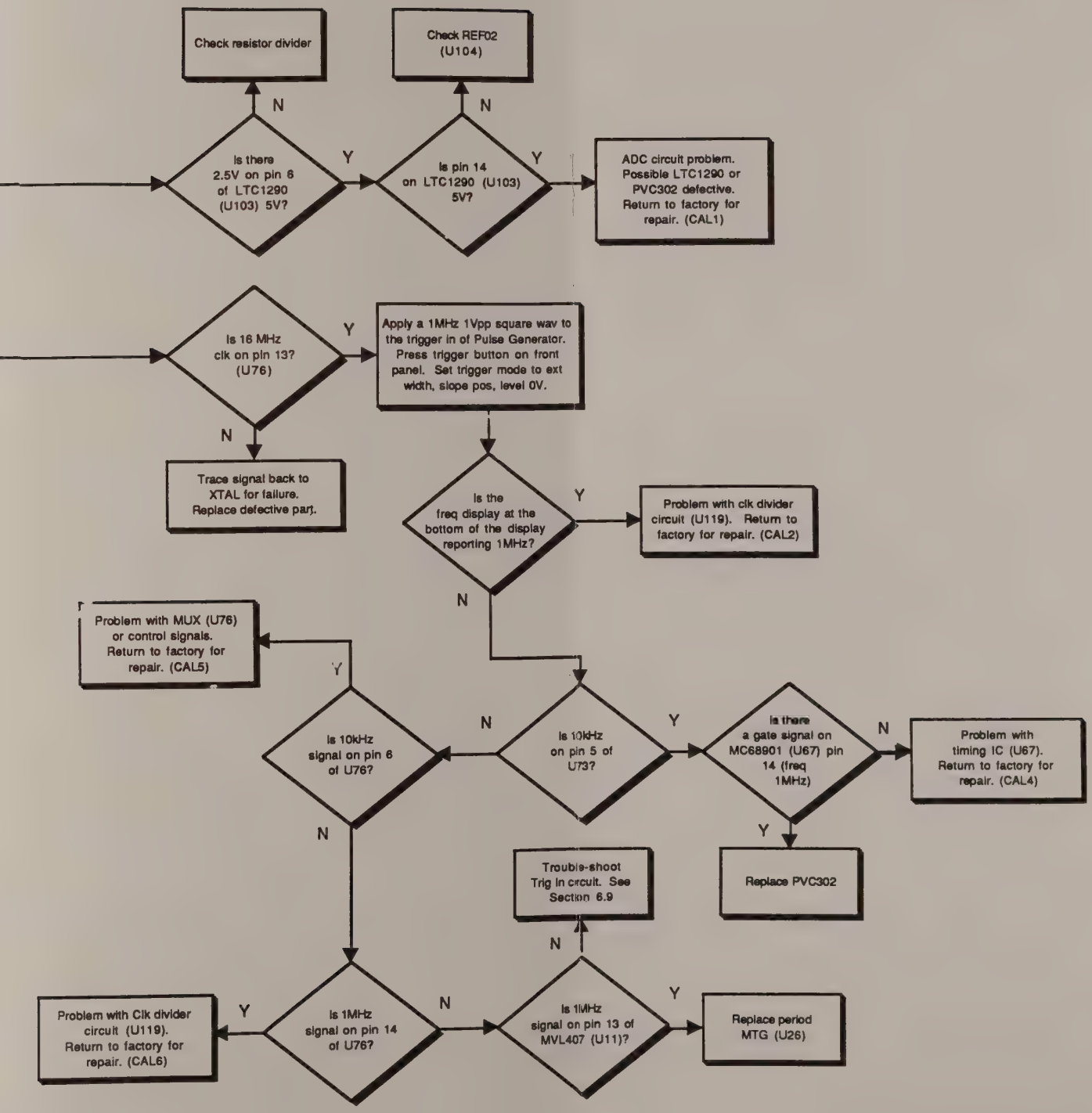
Notes

1

A. Check for designated voltage at test points. Test points are located behind the backplane.

2

A. Press "MORE" key.
B. Select "CAL MSG" on touch screen.


Check resistor divider
Check REF02 (U104)
N
N
Is there 2.5V on pin 6 of LTC1290 (U103) 5V?
Y
Is pin 14 on LTC1290 (U103) 5V?
Y
ADC circuit problem. Possible LTC1290 or PVC302 defective. Return to factory for repair. (CAL1)
Is 16 MHz clk on pin 13? (U76)
Y
Apply a 1MHz 1Vpp square wav to the trigger in of Pulse Generator. Press trigger button on front panel. Set trigger mode to ext width, slope pos, level 0V.
N
Trace signal back to XTAL for failure. Replace defective part.
Is the freq display at the bottom of the display reporting 1MHz?
Y
Problem with clk divider circuit (U119). Return to factory for repair. (CAL2)
N
Problem with MUX (U76) or control signals. Return to factory for repair. (CAL5)
Y
Is 10kHz signal on pin 6 of U76?
N
Is 10kHz on pin 5 of U73?
Y
Is there a gate signal on MC68901 (U67) pin 14 (freq 1MHz)
N
Problem with timing IC (U67). Return to factory for repair. (CAL4)
Y
Replace PVC302
N
Trouble-shoot Trig in circuit. See Section 6.9
N
Problem with Clk divider circuit (U119). Return to factory for repair. (CAL6)
Y
Is 1MHz signal on pin 14 of U76?
N
Is 1MHz signal on pin 13 of MVL407 (U11)?
Y
Replace period MTG (U26)

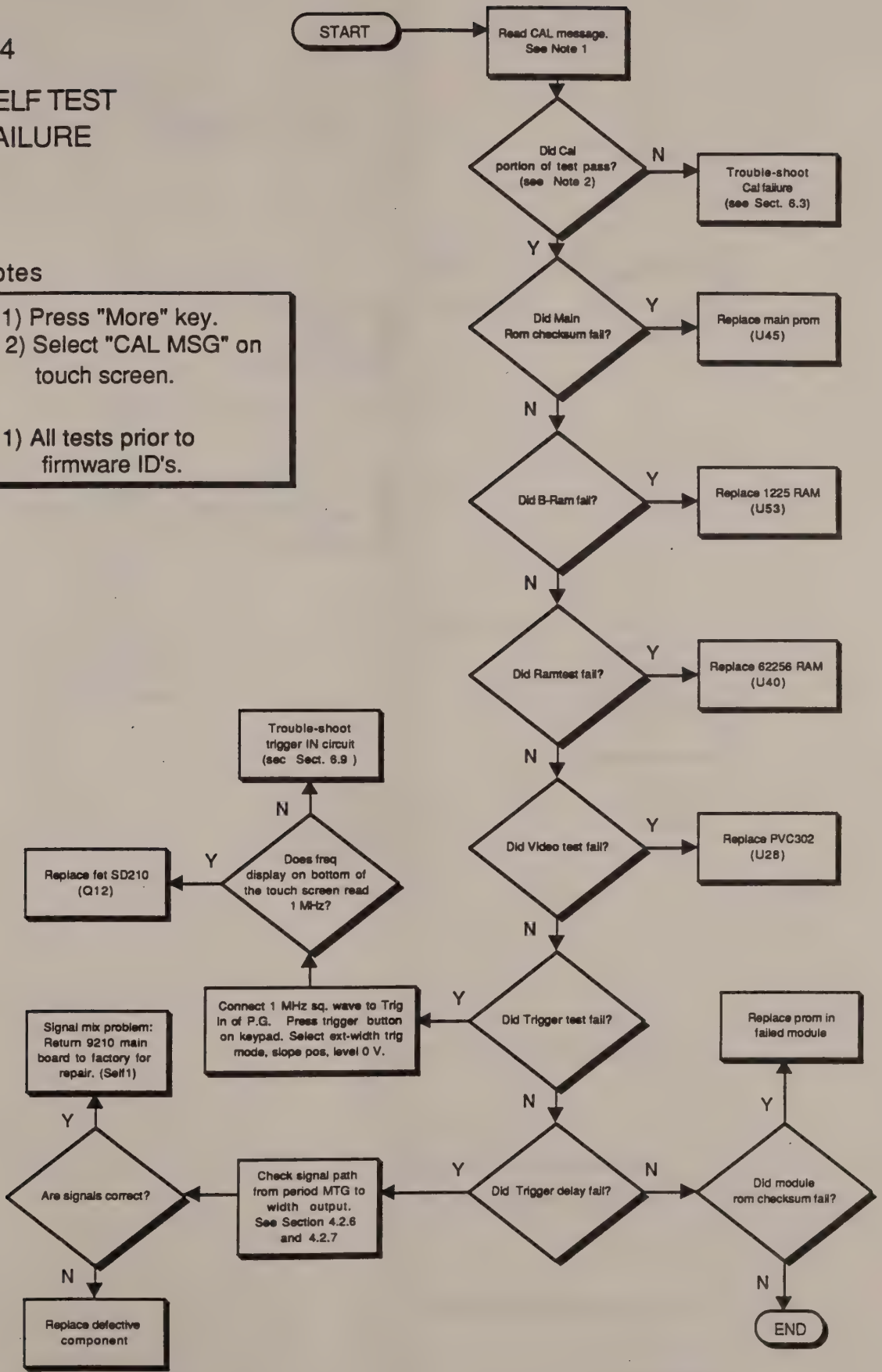
6.4

SELF TEST FAILURE

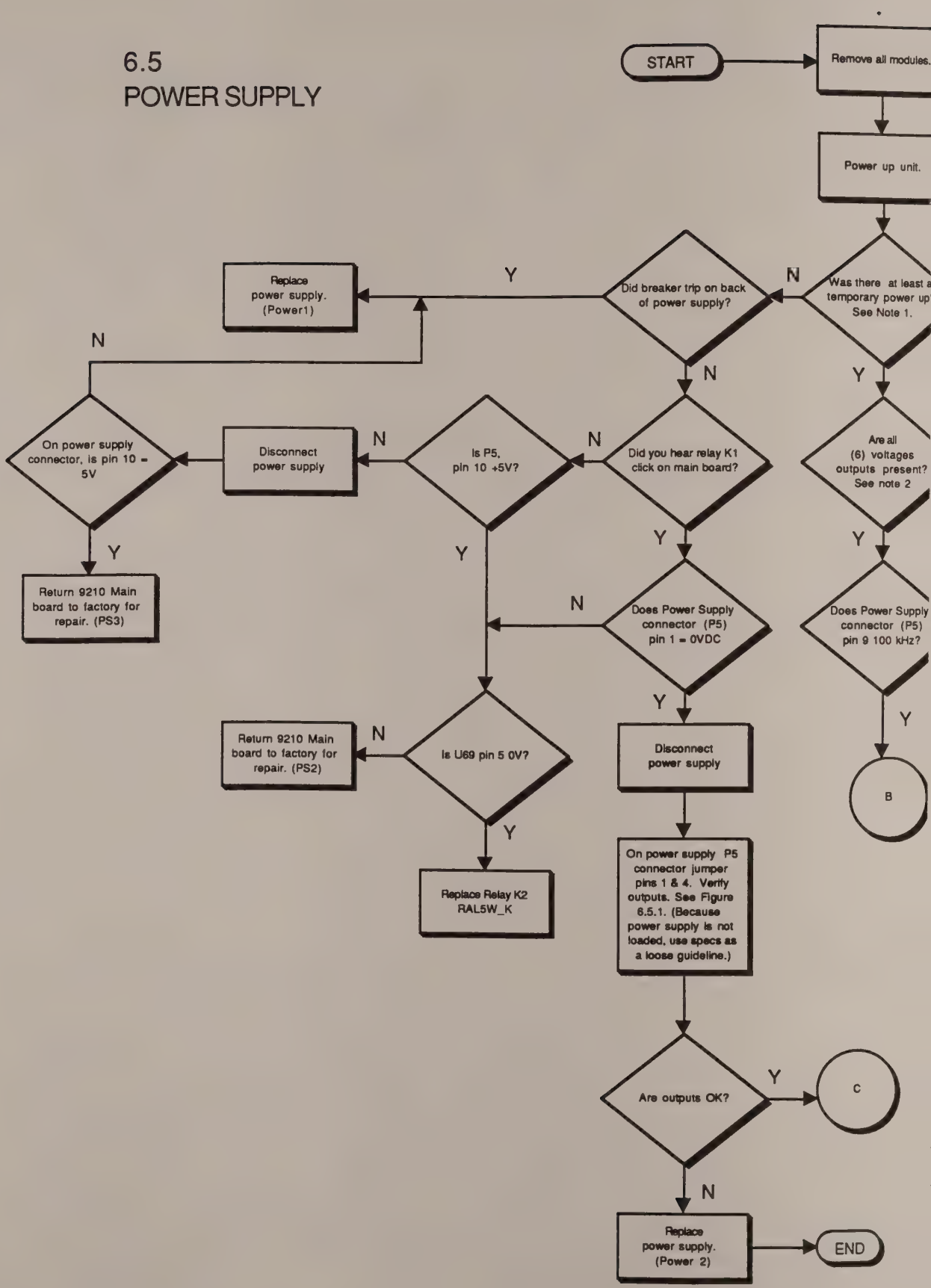
Notes

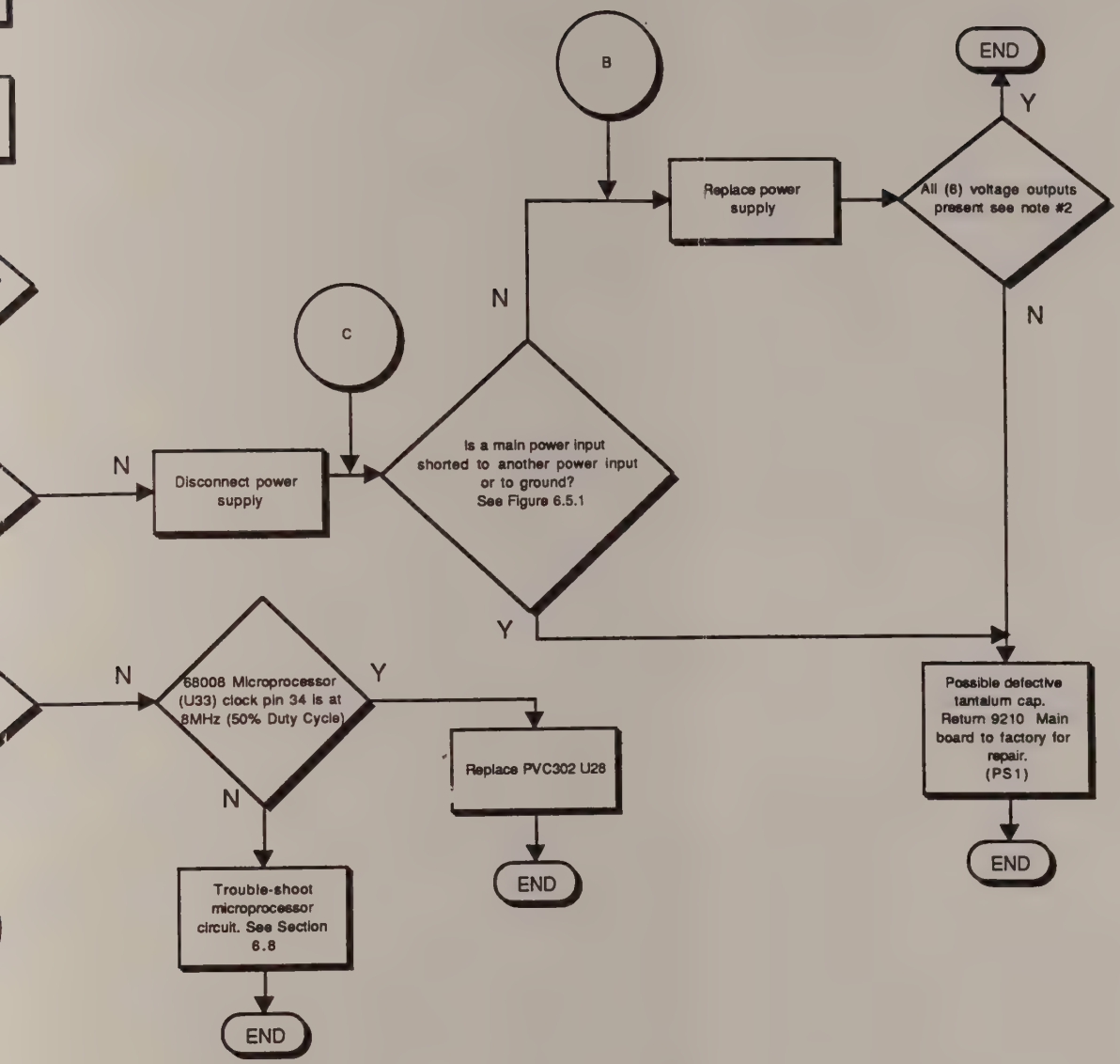
1) 1) Press "More" key.
   2) Select "CAL MSG" on touch screen.

2) 1) All tests prior to firmware ID's.



6.5
POWER SUPPLY





Note 1) Cooling fans come on then shut off.
2) Check for designated voltages at test points. Test points located behind backplane. Verify against specs in Figure 6.5.1

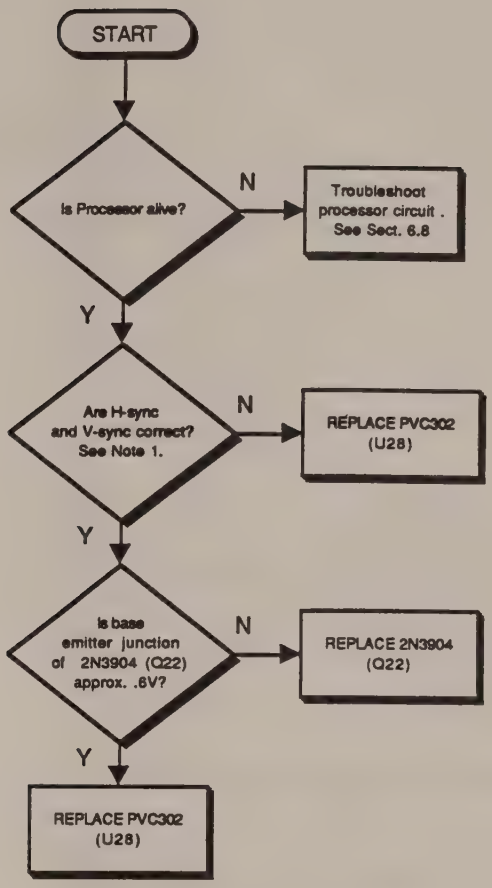
Power Supply Connector (P5) Pinout

PIN	SIGNAL	SPEC.
1	Remote on/off	0v = on
2	-24v	± .12v
3	+24v	± .12v
4	RTN	0v
5	+15v	± .075v
6	RTN	0v
7	-5.2v	± .025v
8	+5v	± .025v
9	Ext Freq.	100 Khz
10	+5 Bias	+5v
11	RTN	0v
12	RTN	0v
13	-15v	± .075v
14	RTN	0v
15	-5.2v	± .025v
16	+5v	± .025v

Power Supply Connector

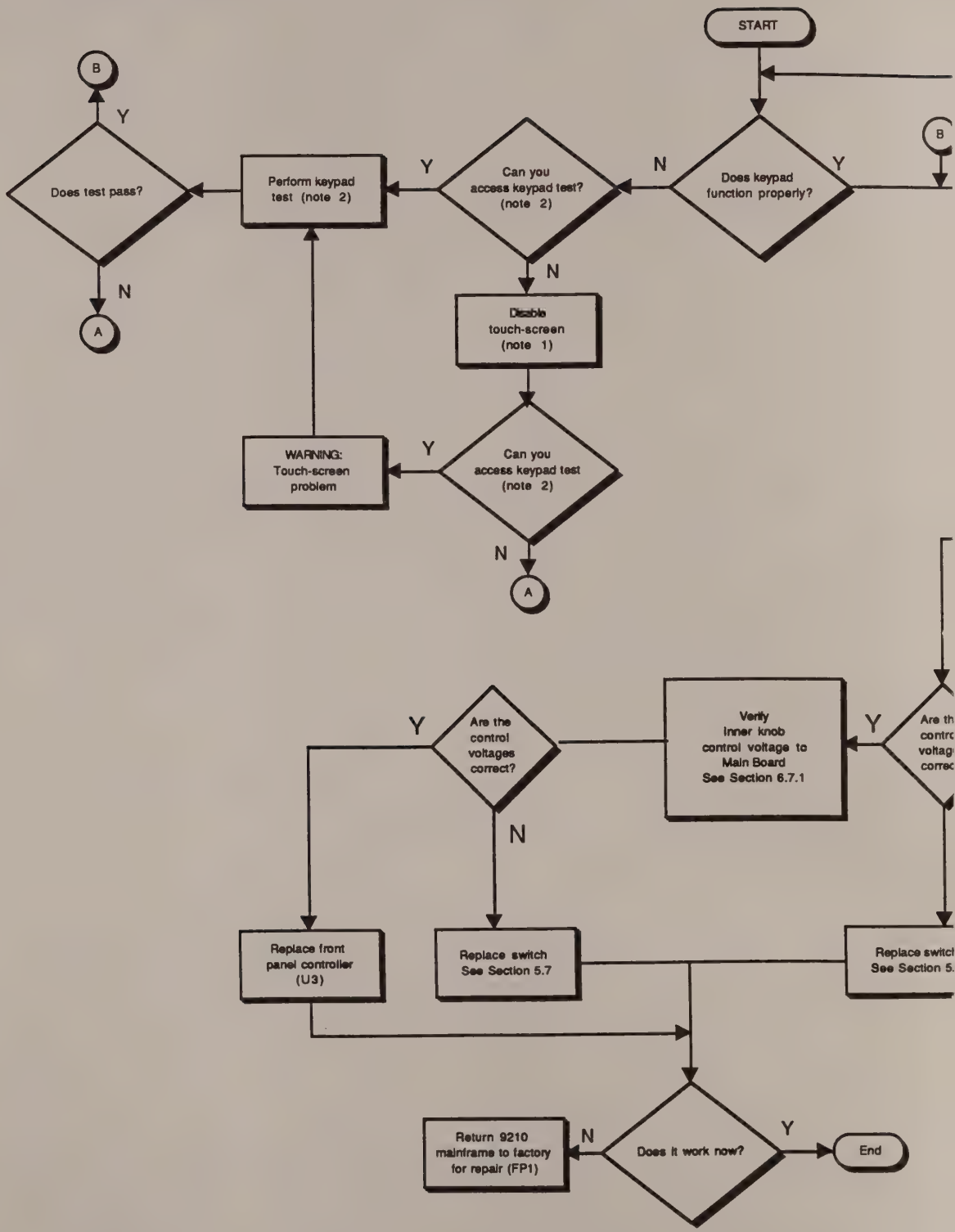
Figure 6.5.1 Power Supply Connector (P5) pinout

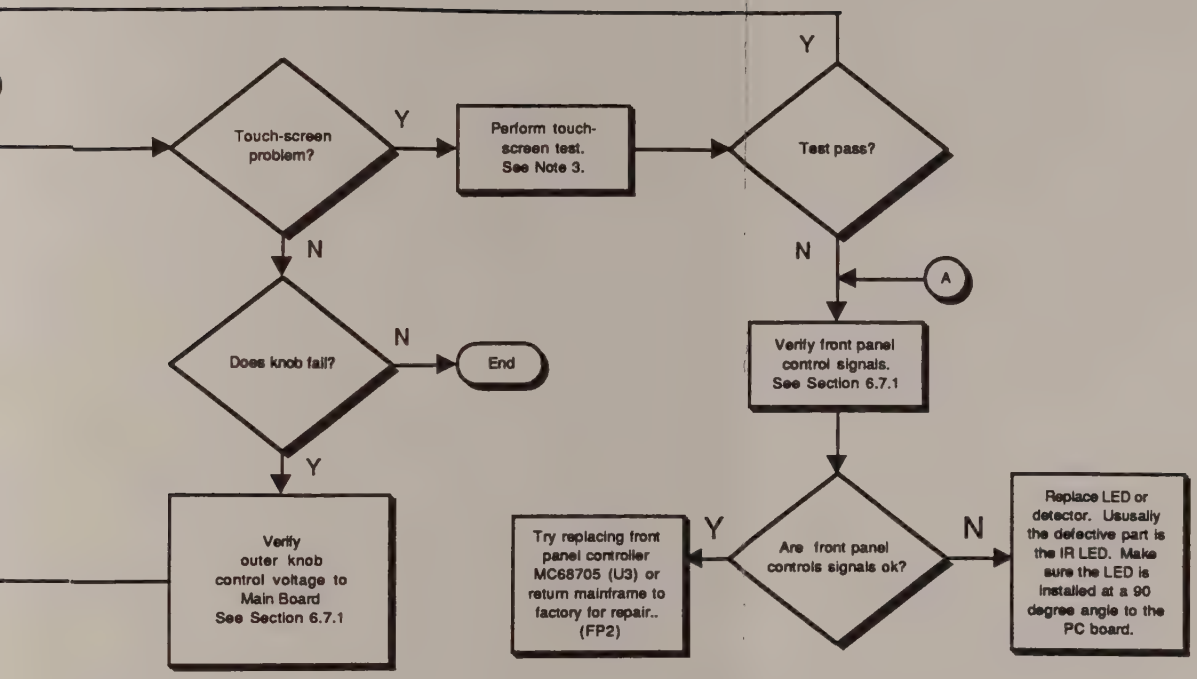
6.6 VIDEO SECTION



Note 1) Horizontal Sync Rate 21.98 kHz (45.5 uS)
Horizontal Sync Width 4.5 us
Vertical Sync rate 57.09 Hz (17.52ms)
Vertical Sync width 682.5 us

6.7
FRONT PANEL





Notes:
1) A) Shut off mainframe.
   B) Block one of the touch CRT keys by placing a finger on the screen.
   C) Turn on the unit.
   D) Block the CRT keys until unit begins to calibrate. (Approx. 15 seconds).
2) A) Press the "More" key.
   B) Select "Test" on the touch screen.
   C) Select "Key Test" on touch screen.
   D) Press all of the keys one at a time. The image of the key on the screen should light up.
3) A) Press the "More" key.
   B) Make sure touch CRT is on (may be menu in Config menu depending on firmware version).
   C) Press the "More" key.
   D) Select "Test" on the touch screen.
   E) Select "Touch Test" on the touch screen.
   F) Press the keys one at a time and the key pressed should light up.

6.7.1 Front Panel Control Signals

It is recommended to read section 4.1, Front Panel Board, prior to troubleshooting the Front Panel.

The Front Panel controller scans the front panel for any interaction. A programmable trigger (TP2 see fig. 6.7.3) is available to assist in troubleshooting the Touch CRT circuit. The trigger is programmed by pressing a number (1-9) on the keypad. The key pressed corresponds to the Touch CRT LED drive and read pair.

The Touch Screen Column (TSC) and Touch Screen Row (TSR) drive signals begin on the falling edge of the programmable trigger (TP2) as shown in figure 6.7.1.

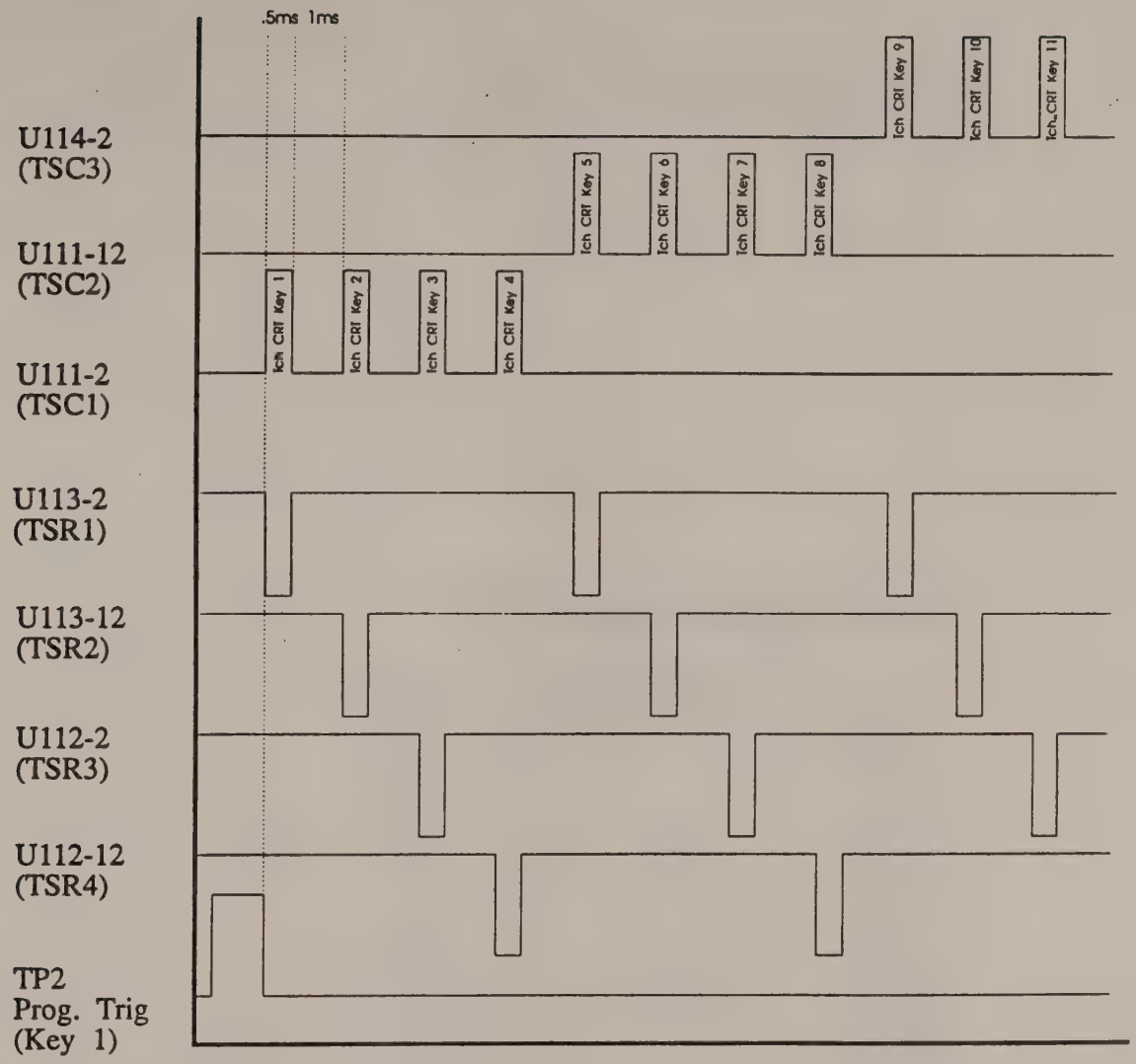
An example of the Touch CRT Key drive signals with Touch CRT Key 1 selected can be found in figure 6.7.2.

An example of the Touch CRT Key Detector (DET) signals can be found in figure 6.7.4.

The front panel knobs control a voltage that is read by the Front Panel Controller.

An example of the control voltages from the inner knob (fine adjustment) can be found in figure 6.7.5.

An example of the control voltages from the outer knob (coarse adjustment) can be found in figure 6.7.6.

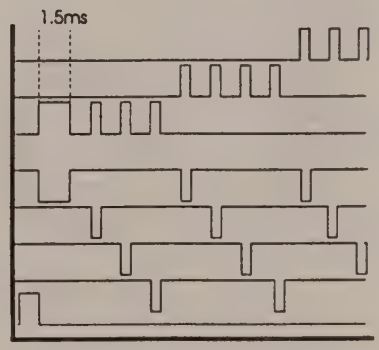


F6.7.1 Touch CRT Control Signal timing (see note 1)

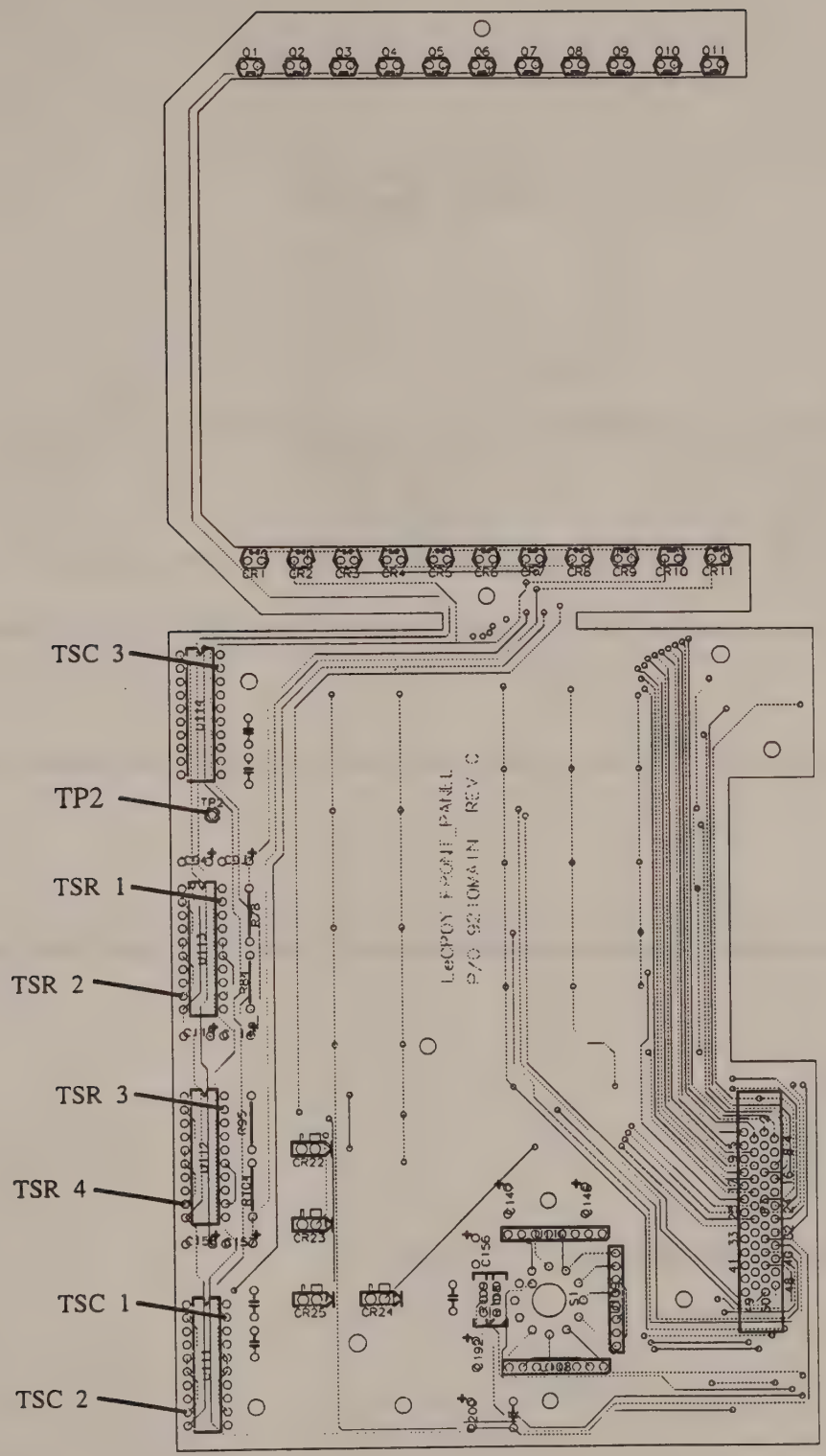
Note 1:

Normal scan timing of the Touch CRT LED signals.

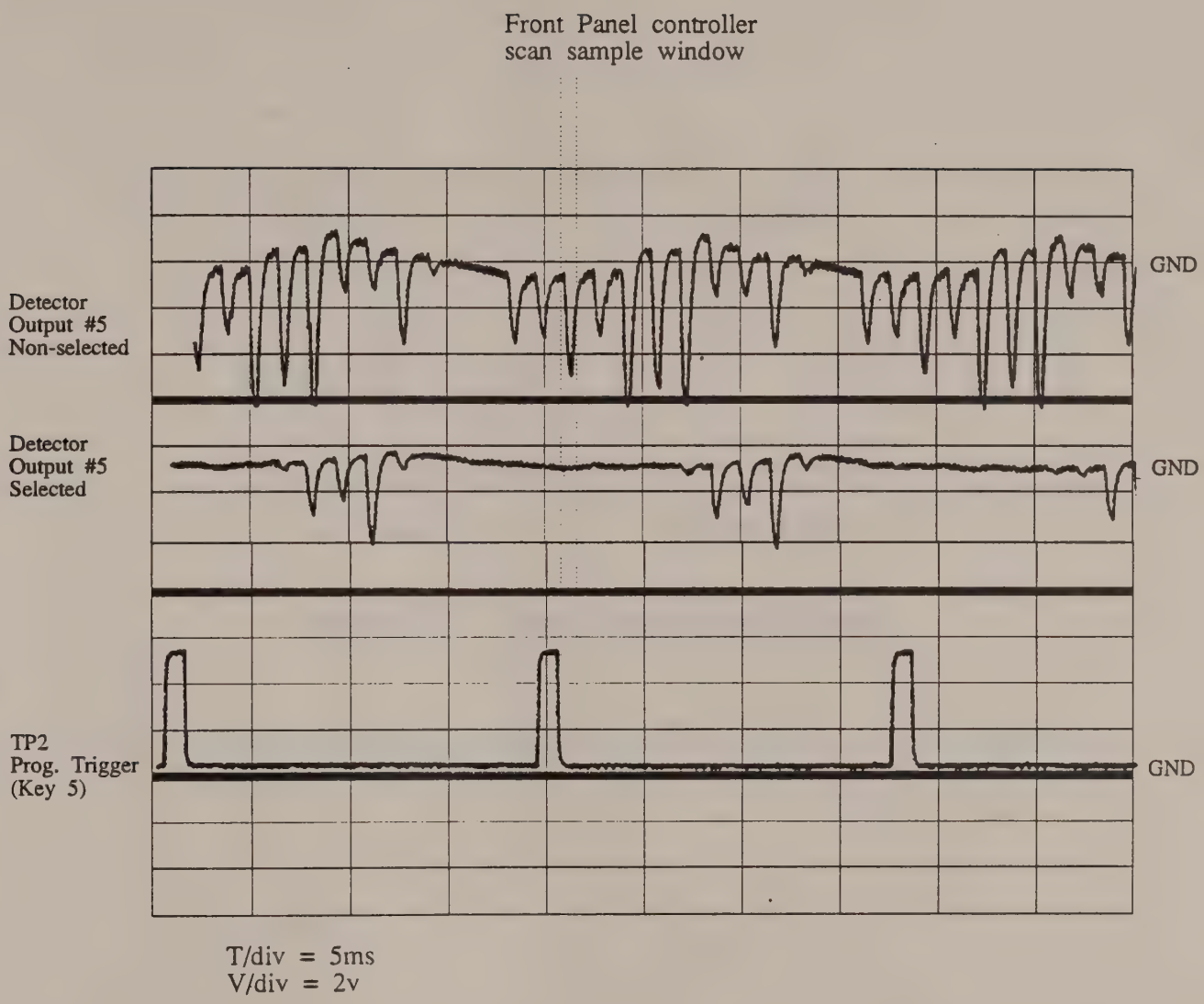
Effect on scan timing when the front panel controller detects an obstructed key. In this example, key #1.



F6.7.2 Touch Key Example



F6.7.3 **Front Panel PC Board** (solder side)



F6.7.4 Touch CRT Key Detector Signals

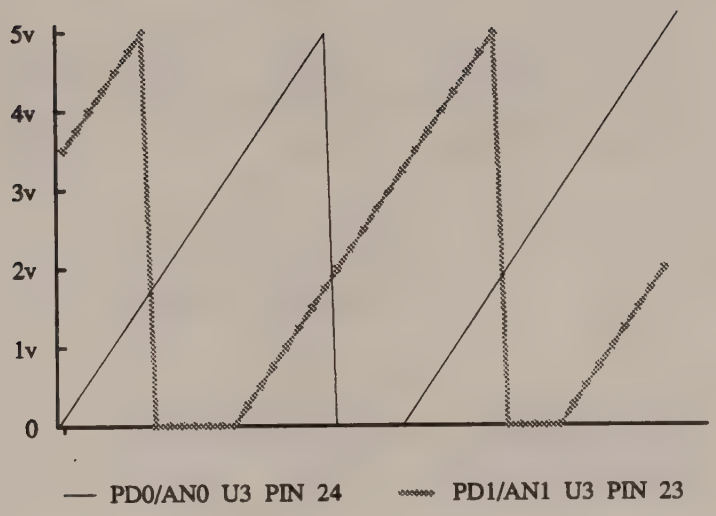


Figure 6.7.5 Inner Knob Control Voltages

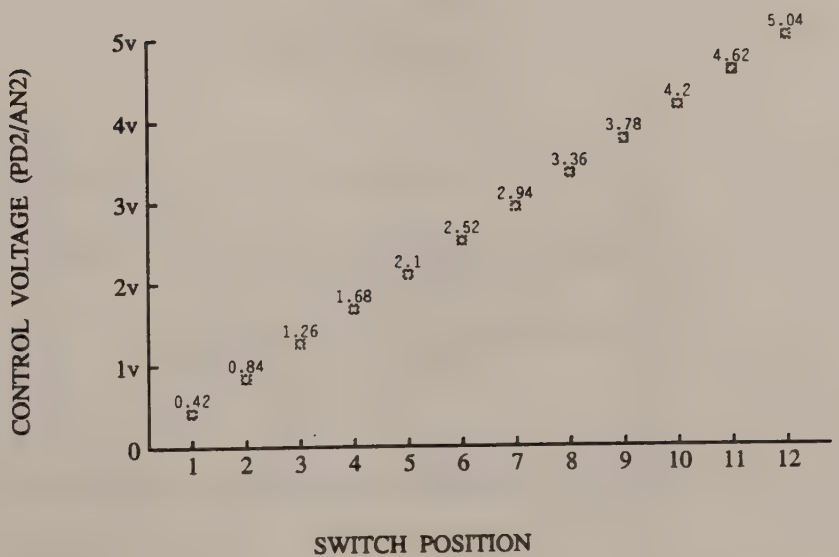
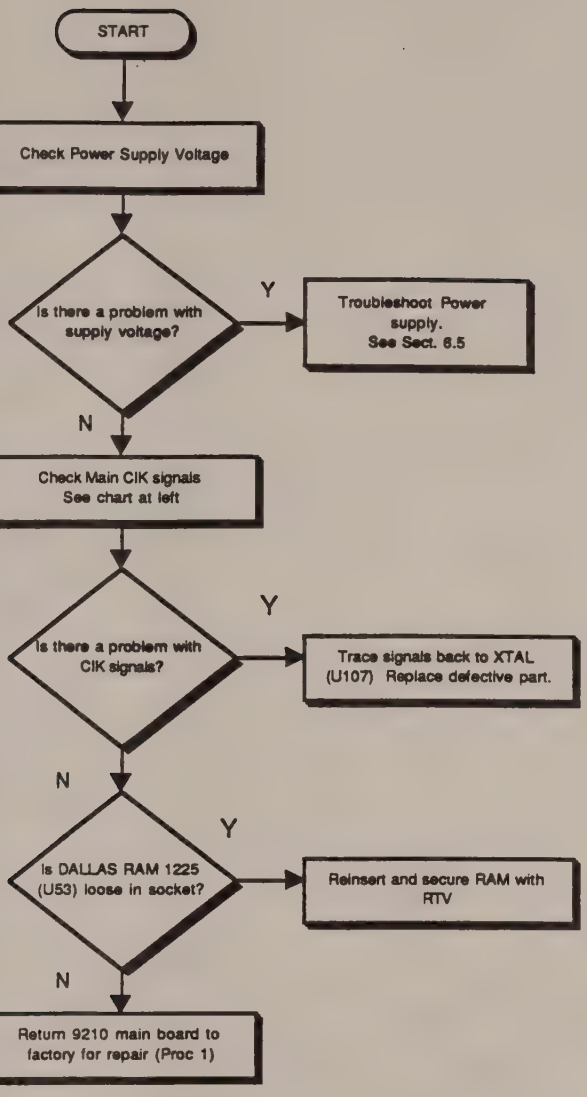


Figure 6.7.6 Outer Knob Control Voltages

6.8
PROCESSOR CIRCUIT

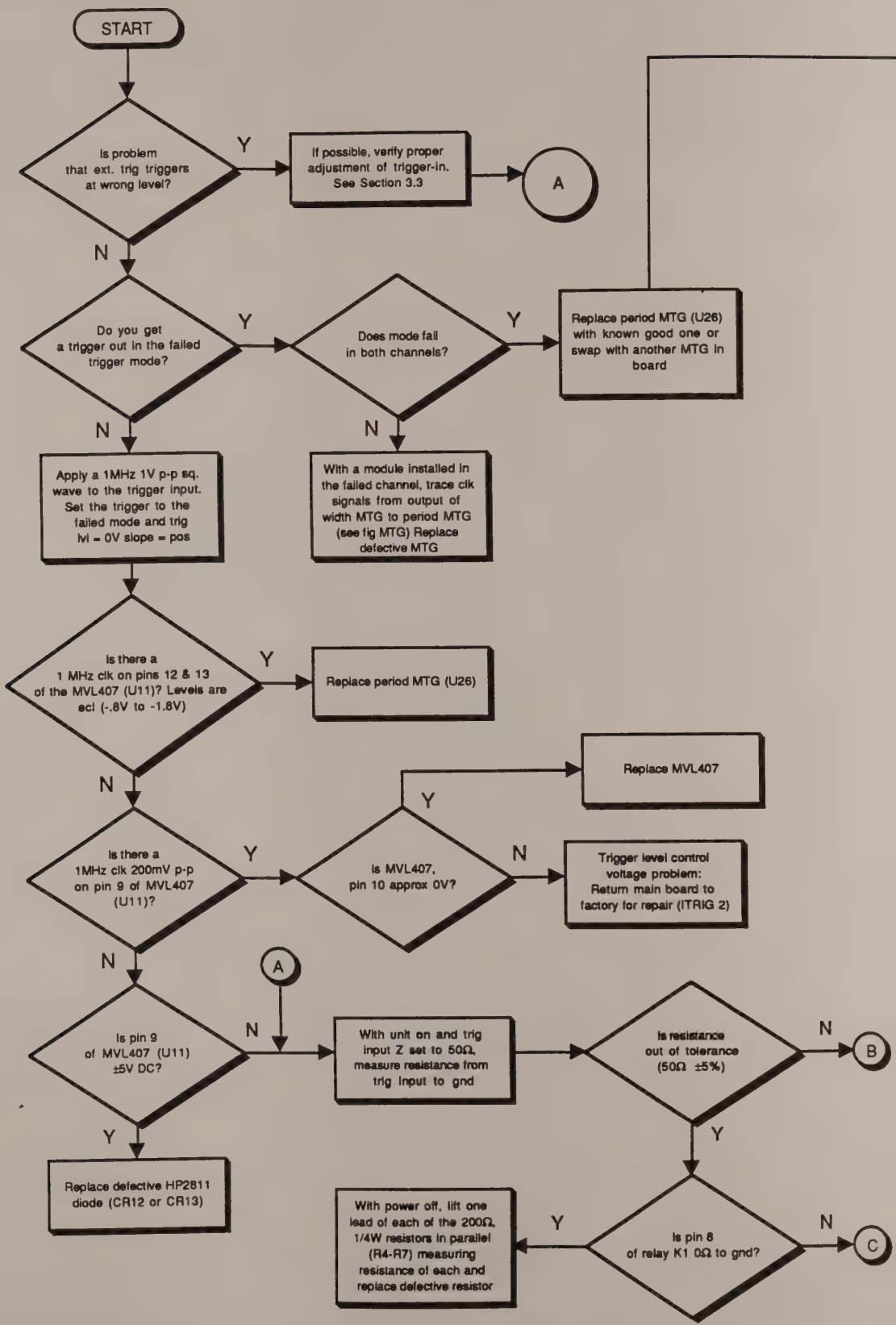
MAIN CLOCK SIGNALS:

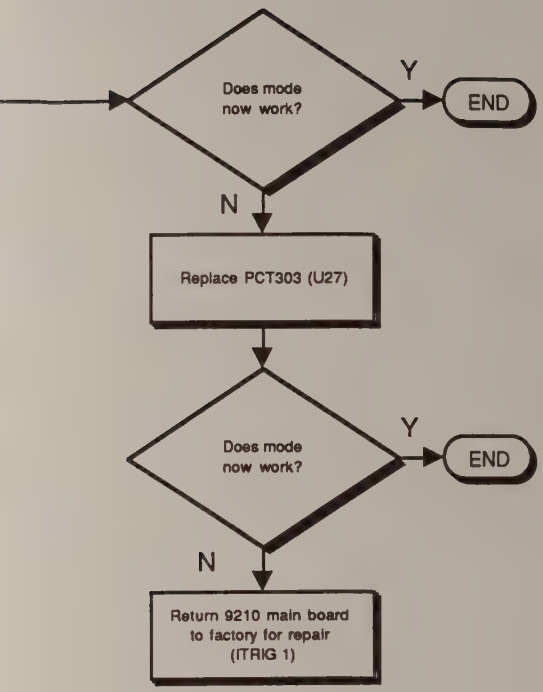
16 MHz CIK	U72	Pin 10
µp CIK (8MHz)	U68	Pin 11
CIK 4 MHz	U67	Pin 17

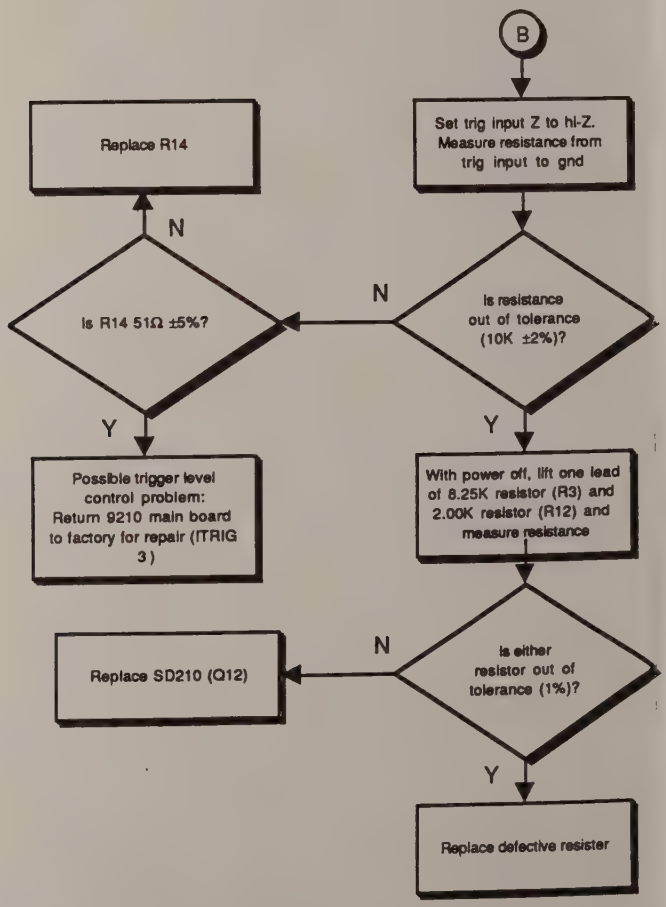


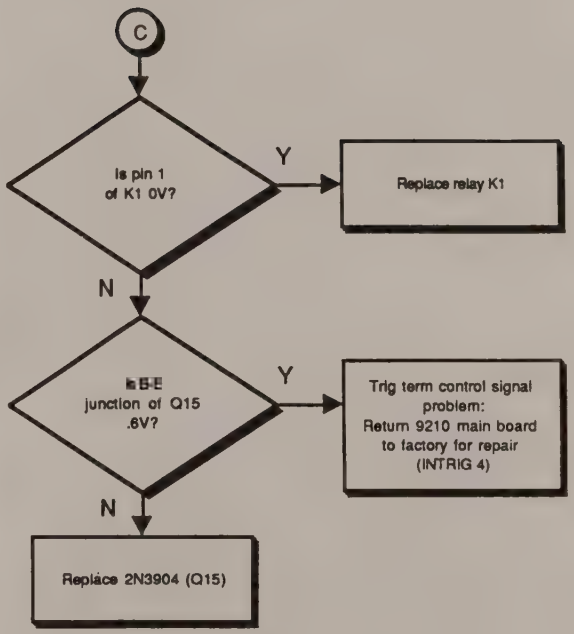
Note 1) Check for designated voltages at test points. Test points are located behind backplane. Verify against specs in Figure 6.5.1

6.9
TRIGGER IN

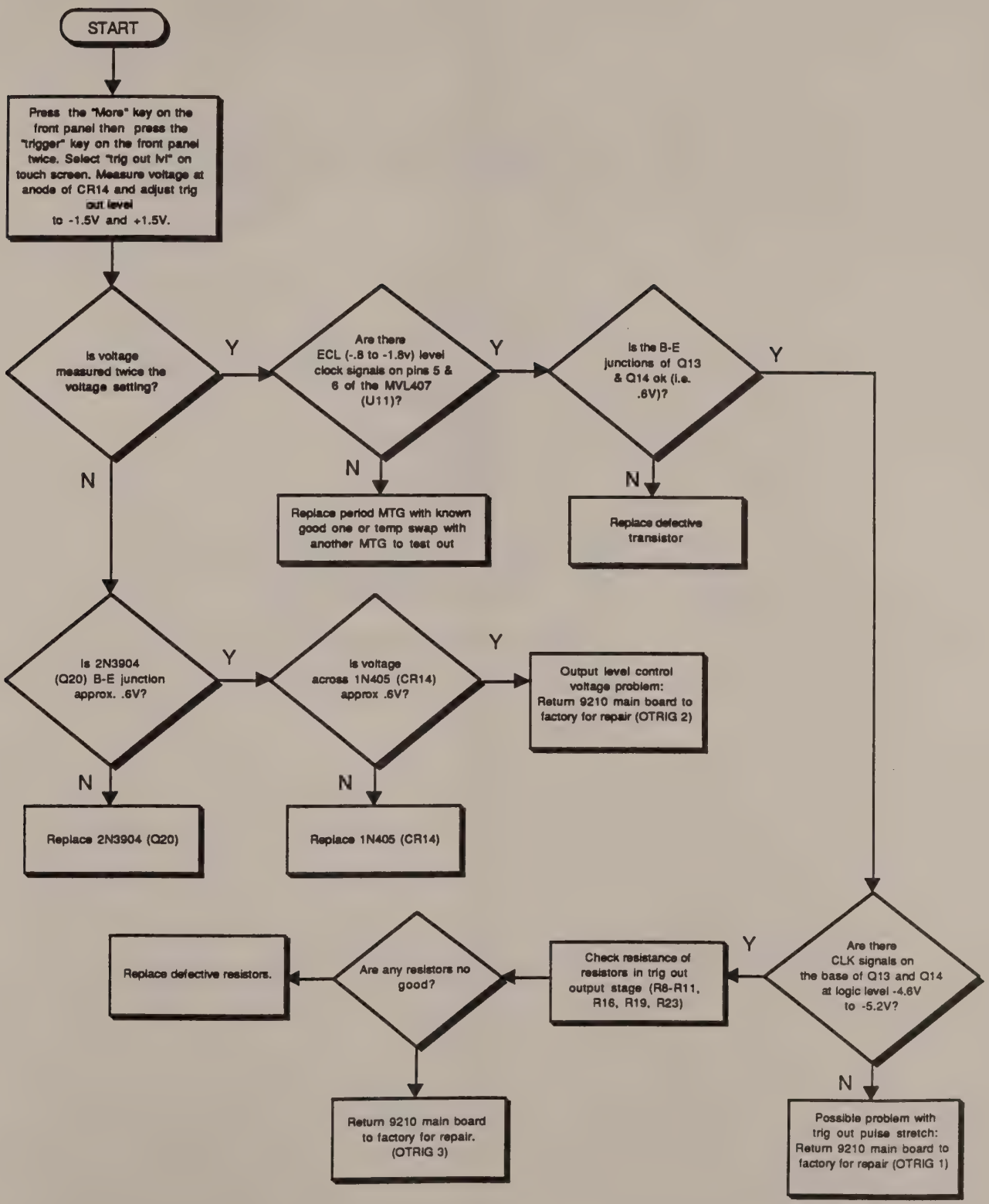



Does mode now work?
Y
END
N
Replace PCT303 (U27)
Does mode now work?
Y
END
N
Return 9210 main board to factory for repair (ITRIG 1)

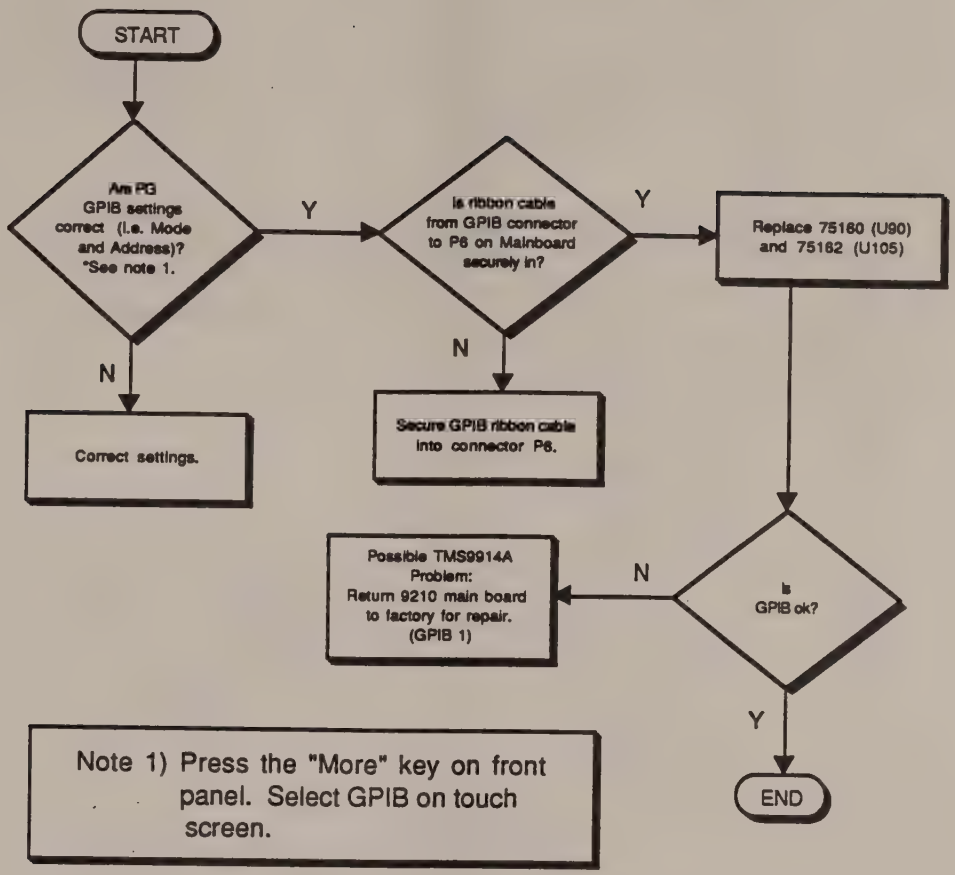

B
Set trig input Z to hi-Z. Measure resistance from trig input to gnd
Is resistance out of tolerance (10K ±2%)?
N
Is R14 51Ω ±5%?
N
Replace R14
Y
Possible trigger level control problem: Return 9210 main board to factory for repair (ITRIG 3)
Y
With power off, lift one lead of 8.25K resistor (R3) and 2.00K resistor (R12) and measure resistance
Is either resistor out of tolerance (1%)?
N
Replace SD210 (Q12)
Y
Replace defective resister


C
Is pin 1 of K1 0V?
Y
Replace relay K1
N
Is B-E junction of Q15 .6V?
Y
Trig term control signal problem: Return 9210 main board to factory for repair (INTRIG 4)
N
Replace 2N3904 (Q15)

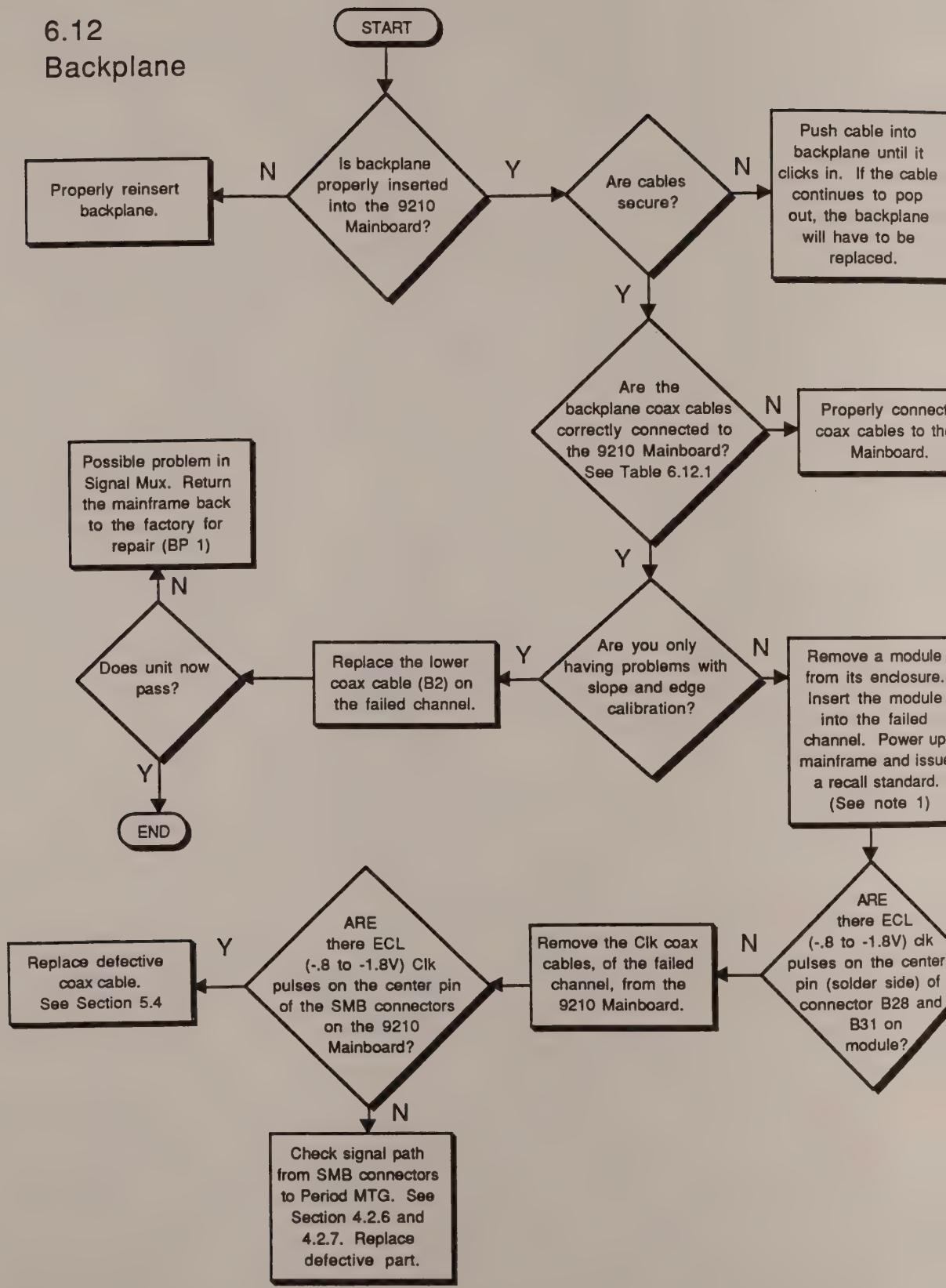
6.10
TRIGGER OUT



6.11
GPIB


START
Are PG GPIB settings correct (I.e. Mode and Address)? *See note 1.
Y
Is ribbon cable from GPIB connector to P6 on Mainboard securely in?
Y
Replace 75160 (U90) and 75162 (U105)
N
Correct settings.
N
Secure GPIB ribbon cable into connector P6.
Possible TMS9914A Problem: Return 9210 main board to factory for repair. (GPIB 1)
N
Is GPIB ok?
Y
END
Note 1) Press the "More" key on front panel. Select GPIB on touch screen.

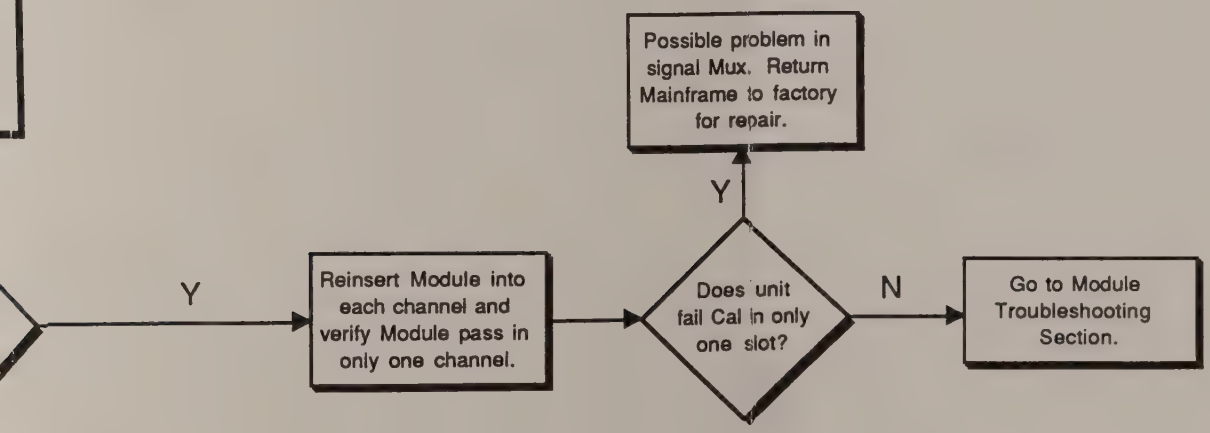
6.12 Backplane

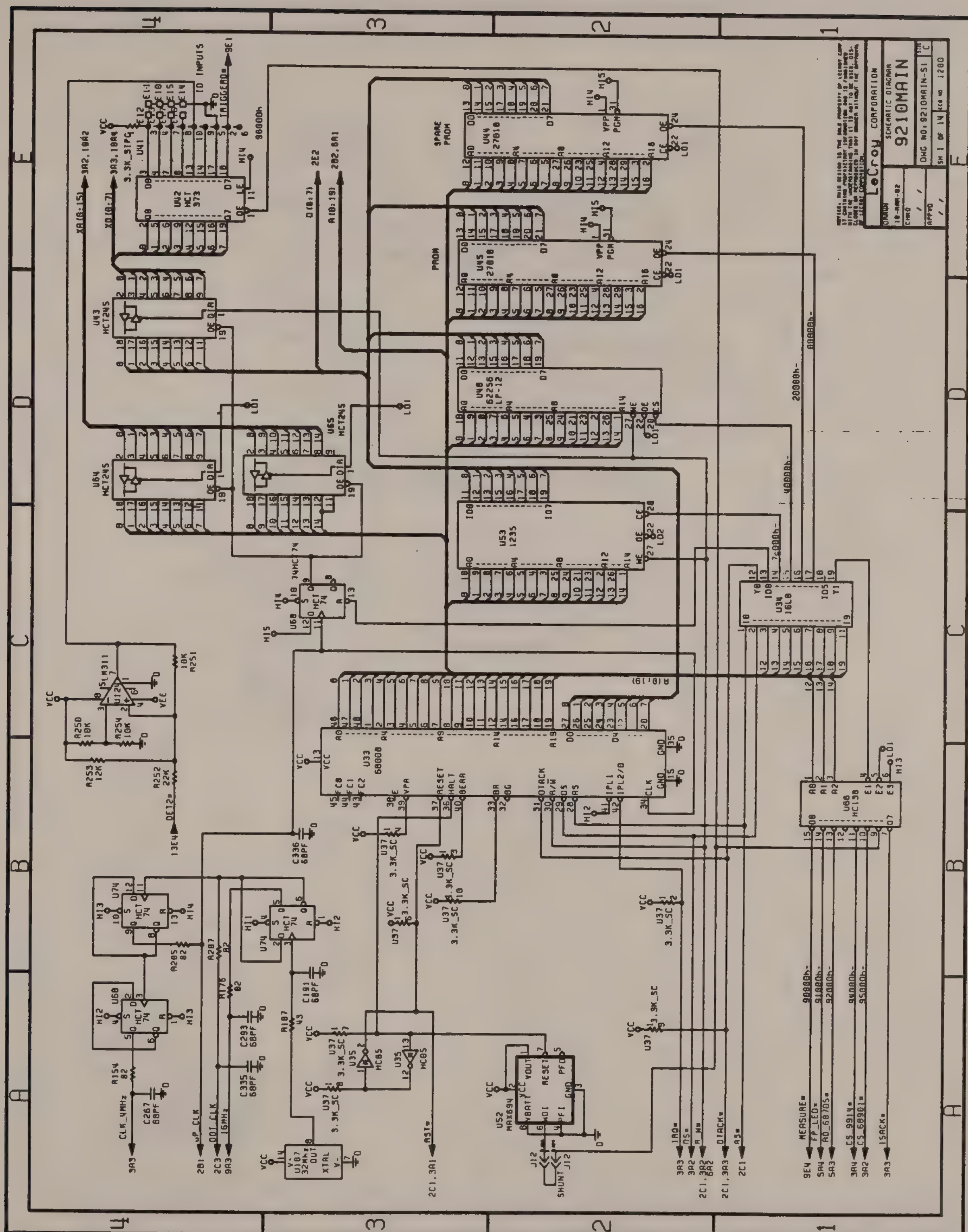


Note 1) A) Press "Recall Setup" on front panel.
B) Select "Standard" on touch screen.
C) Select "Execute" on touch screen.

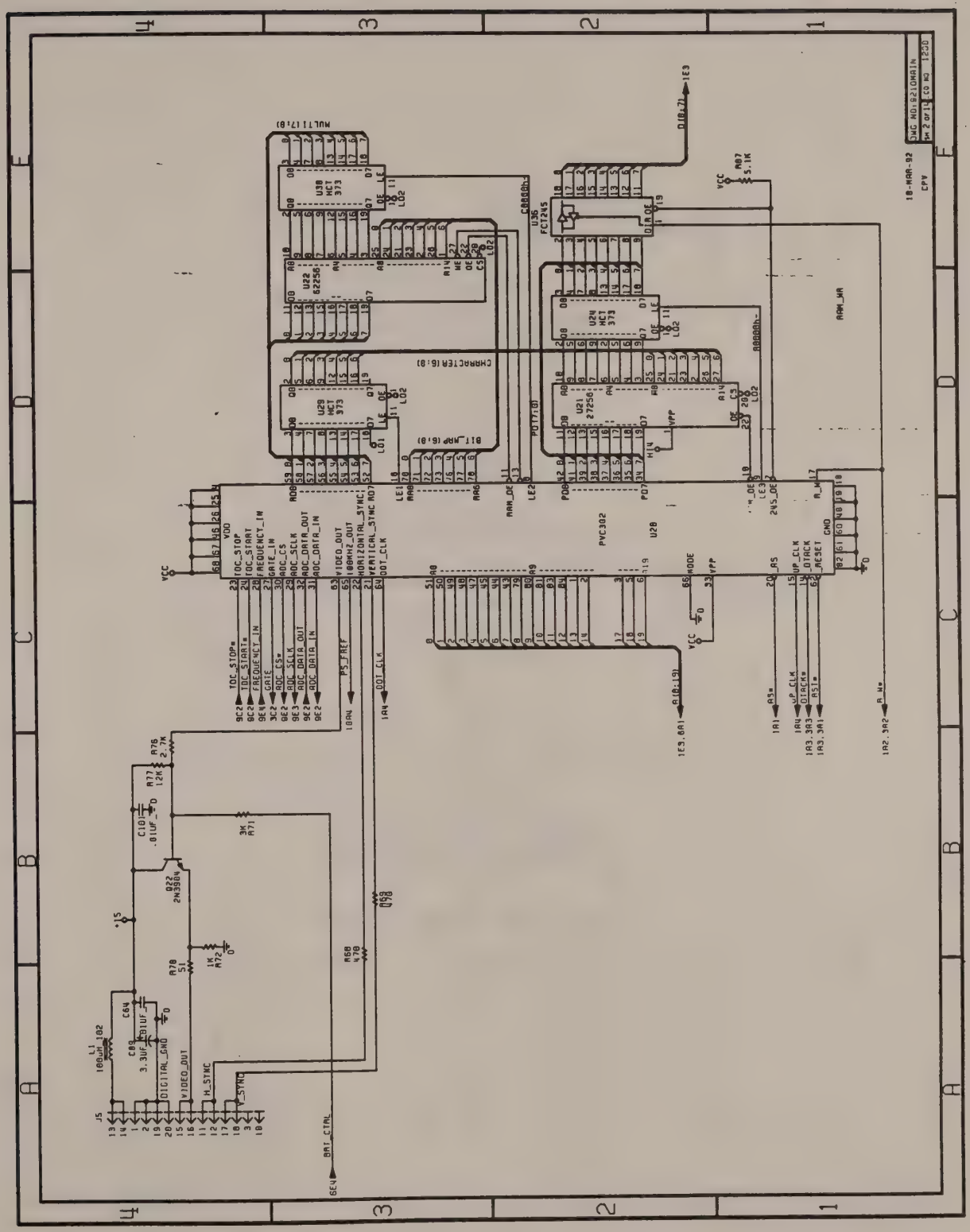
Backplane Cabling : Table 6.12.

	Backplane	9210 Main board
Channel A	B31	JA1 (J10)
	B28	JA2 (J11)
	B5	Not Used
	B2	JA4 (J14)
Channel B	B31	JB1 (J8)
	B28	JB2 (J9)
	B5	Not Used
	B2	JB4 (J15)

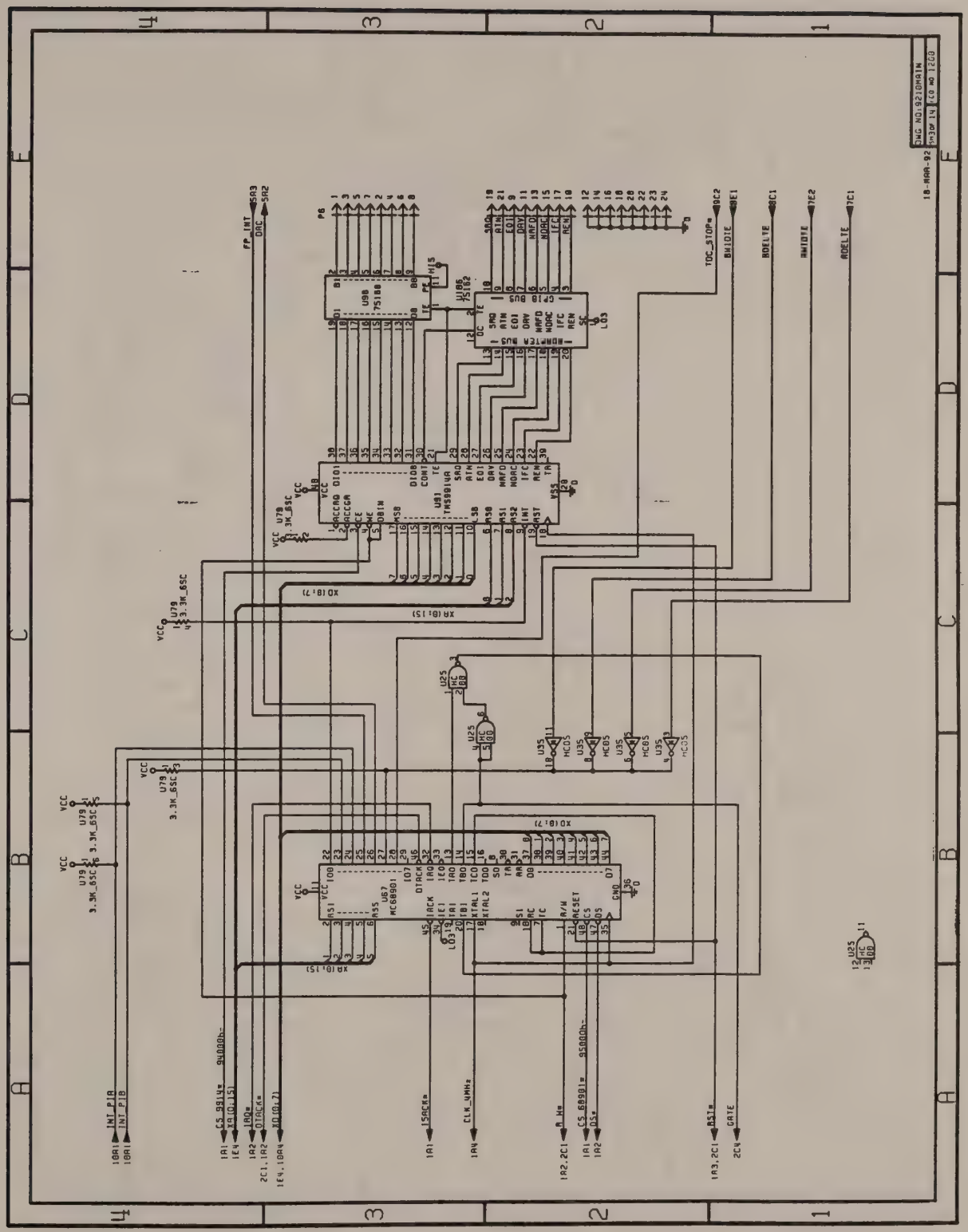




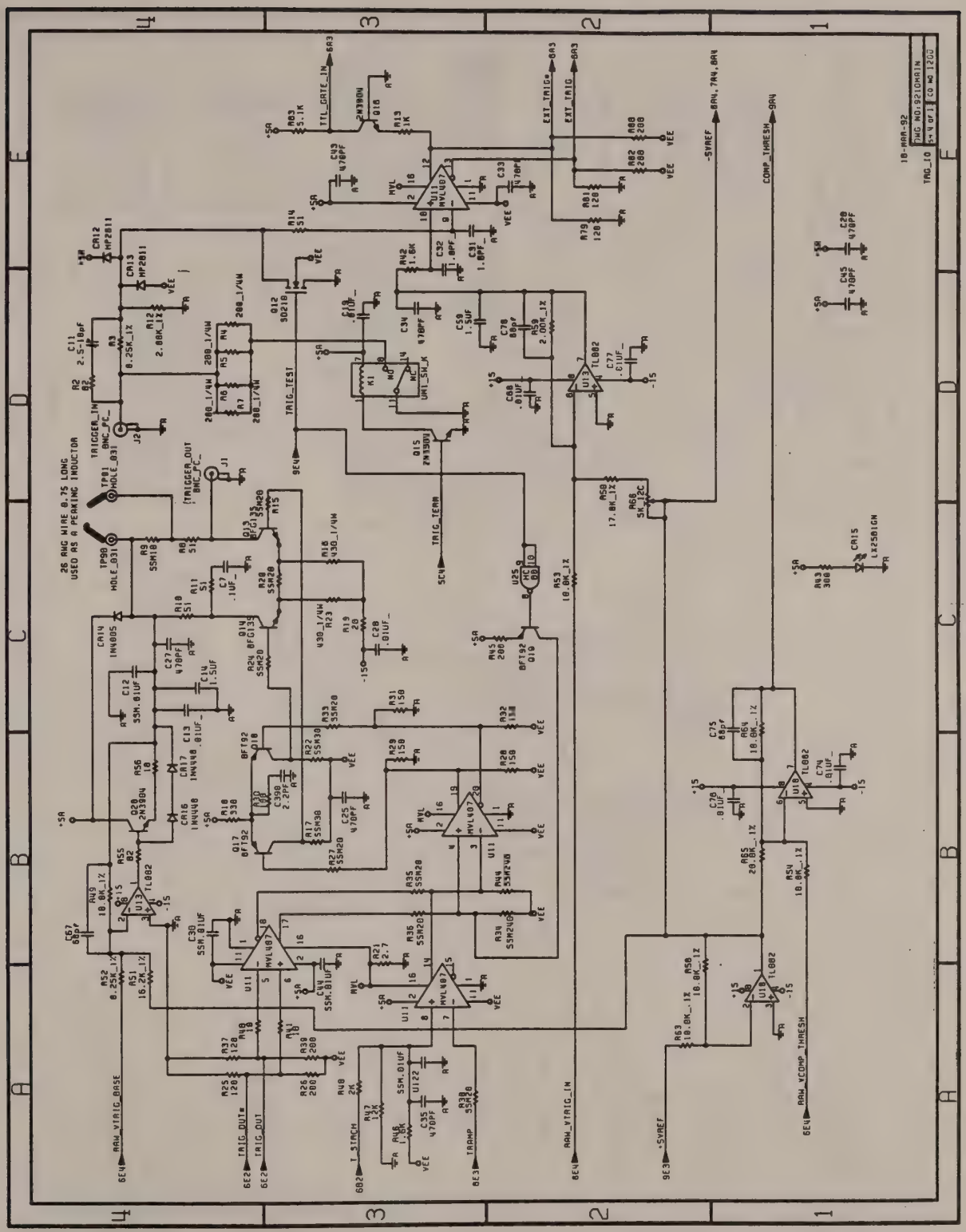
S1 9210 Main Schematics Rev B-1



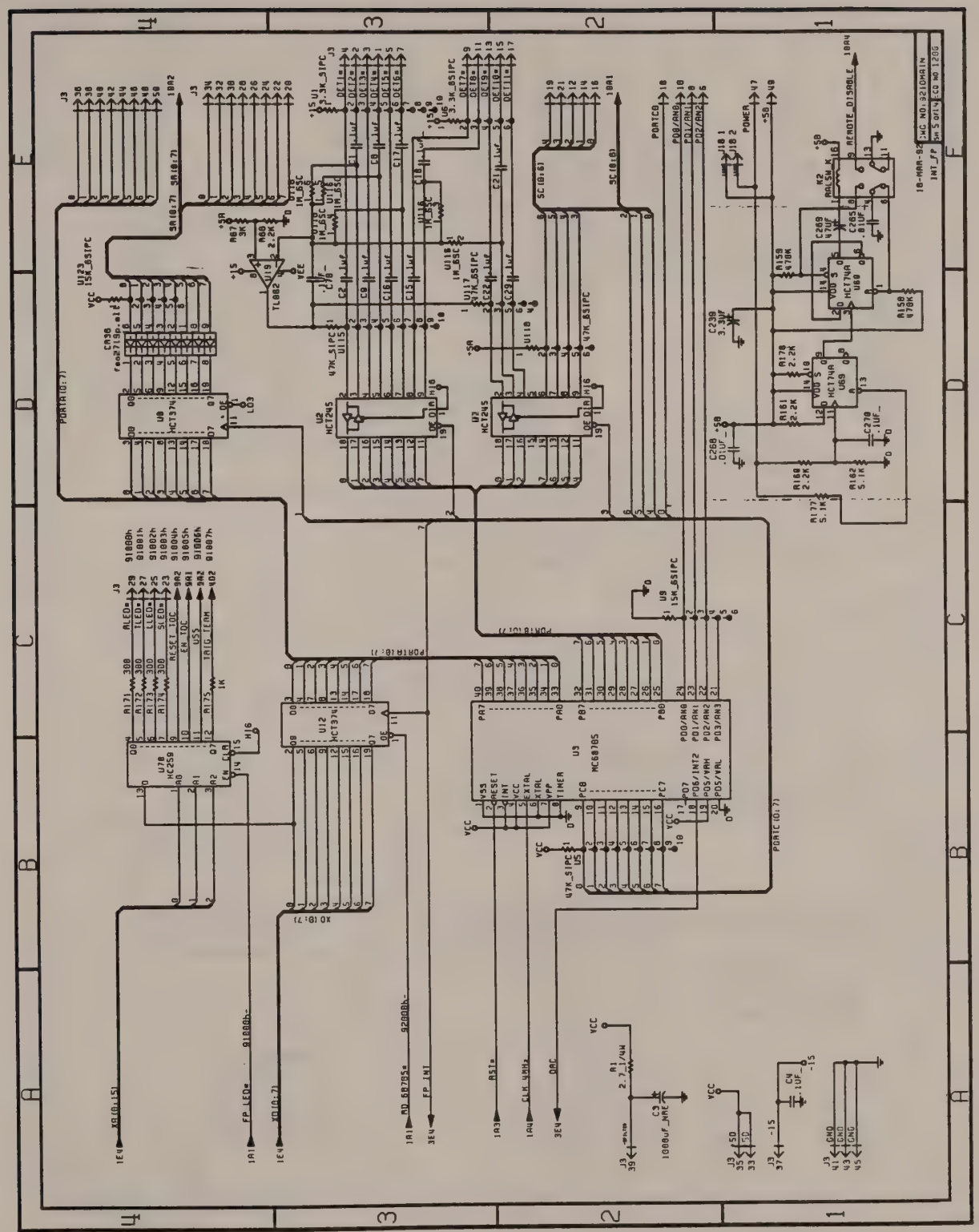
S2 9210 Main Schematics Rev B-2



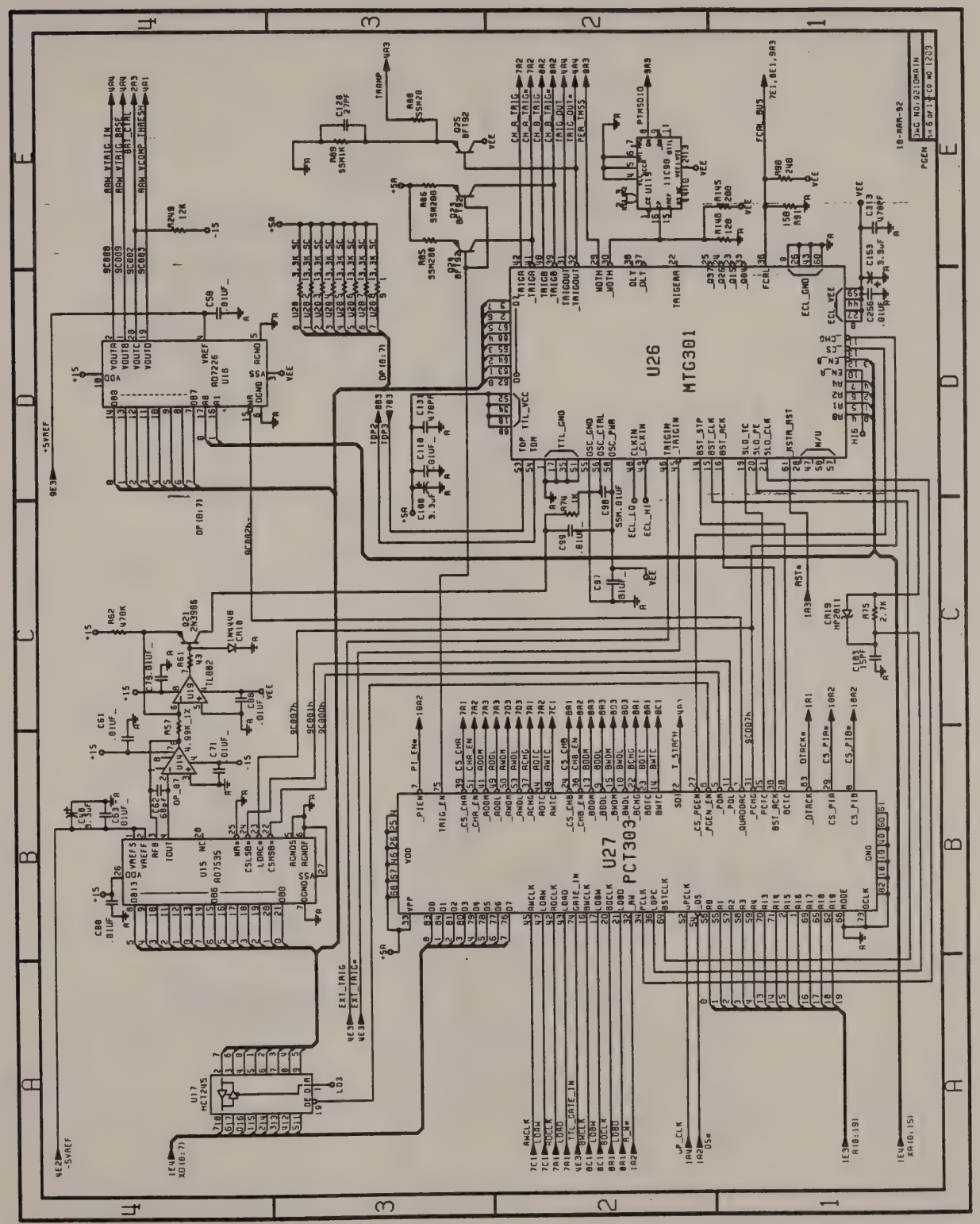
S3 9210 Main Schematics Rev B-3



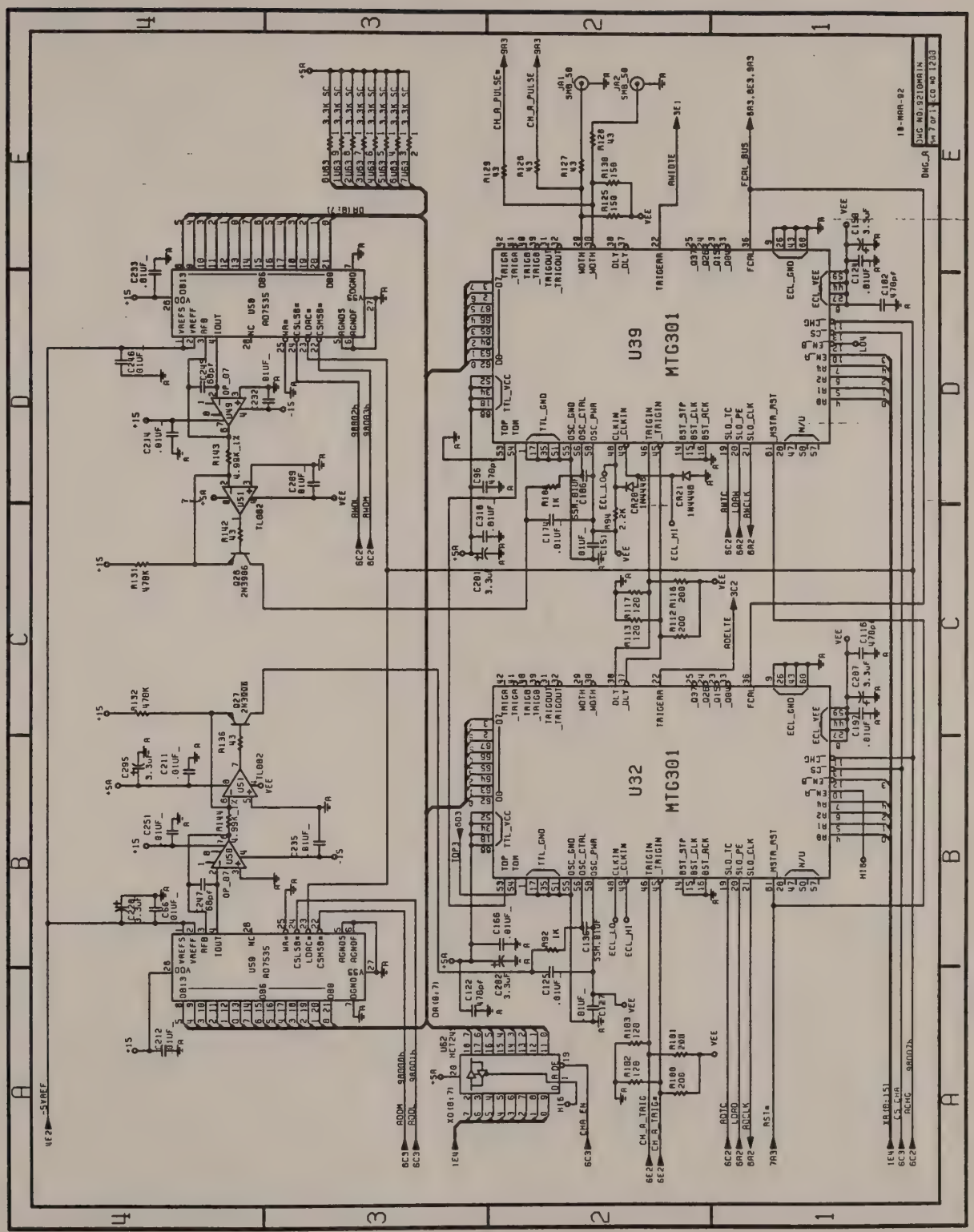
S4 9210 Main Schematics Rev B-4



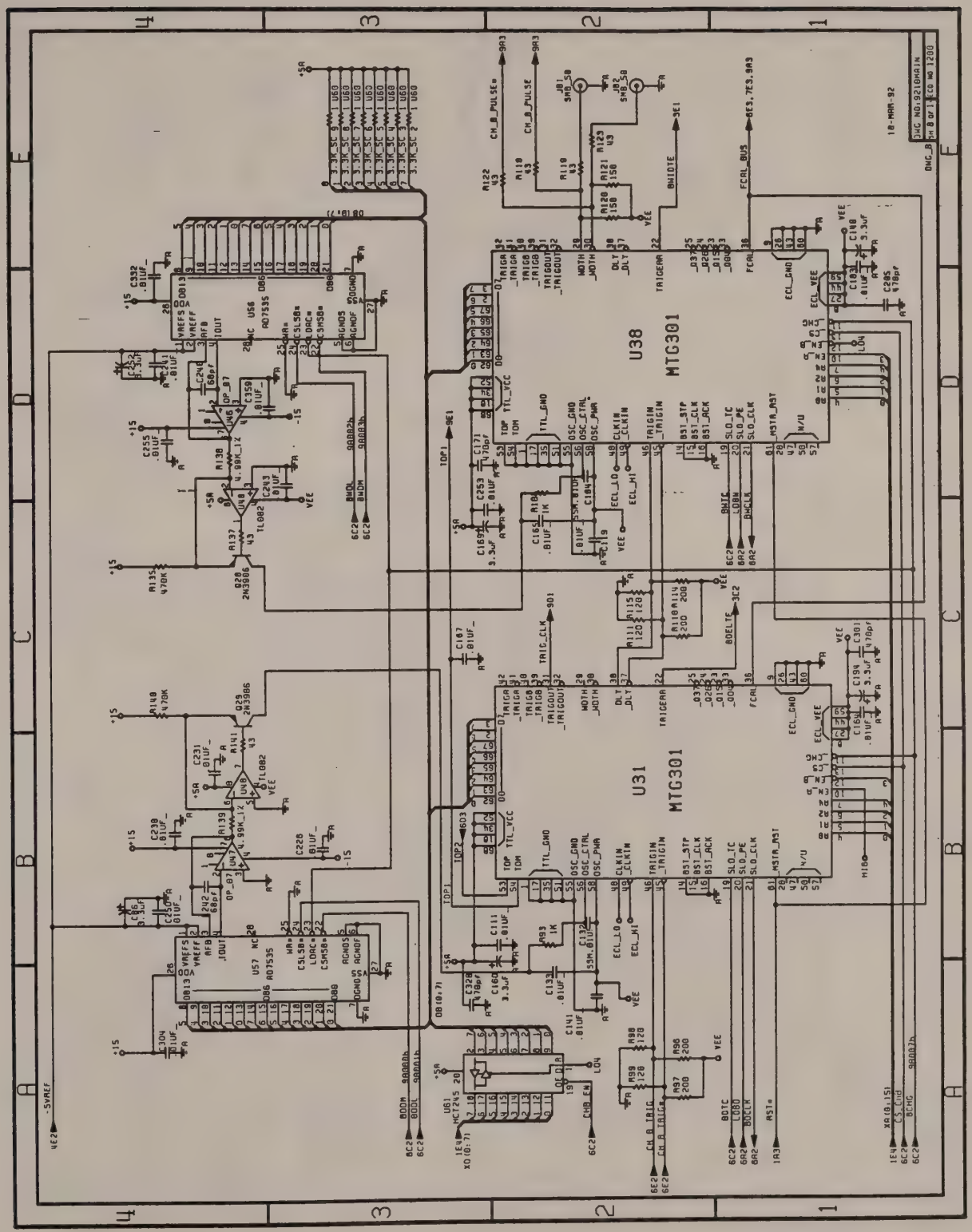
S5 9210 Main Schematics Rev B-5



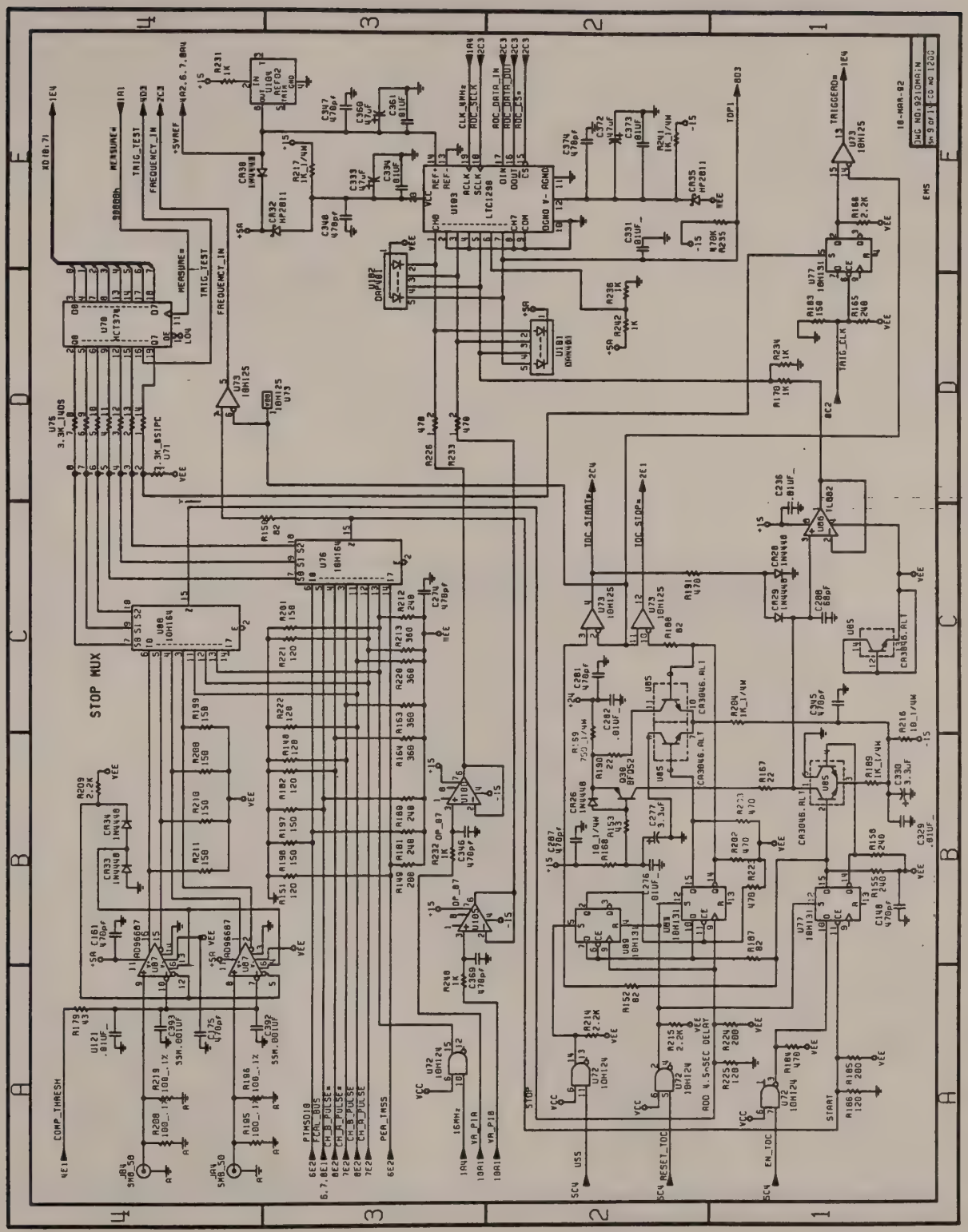
S6 9210 Main Schematics Rev B-6



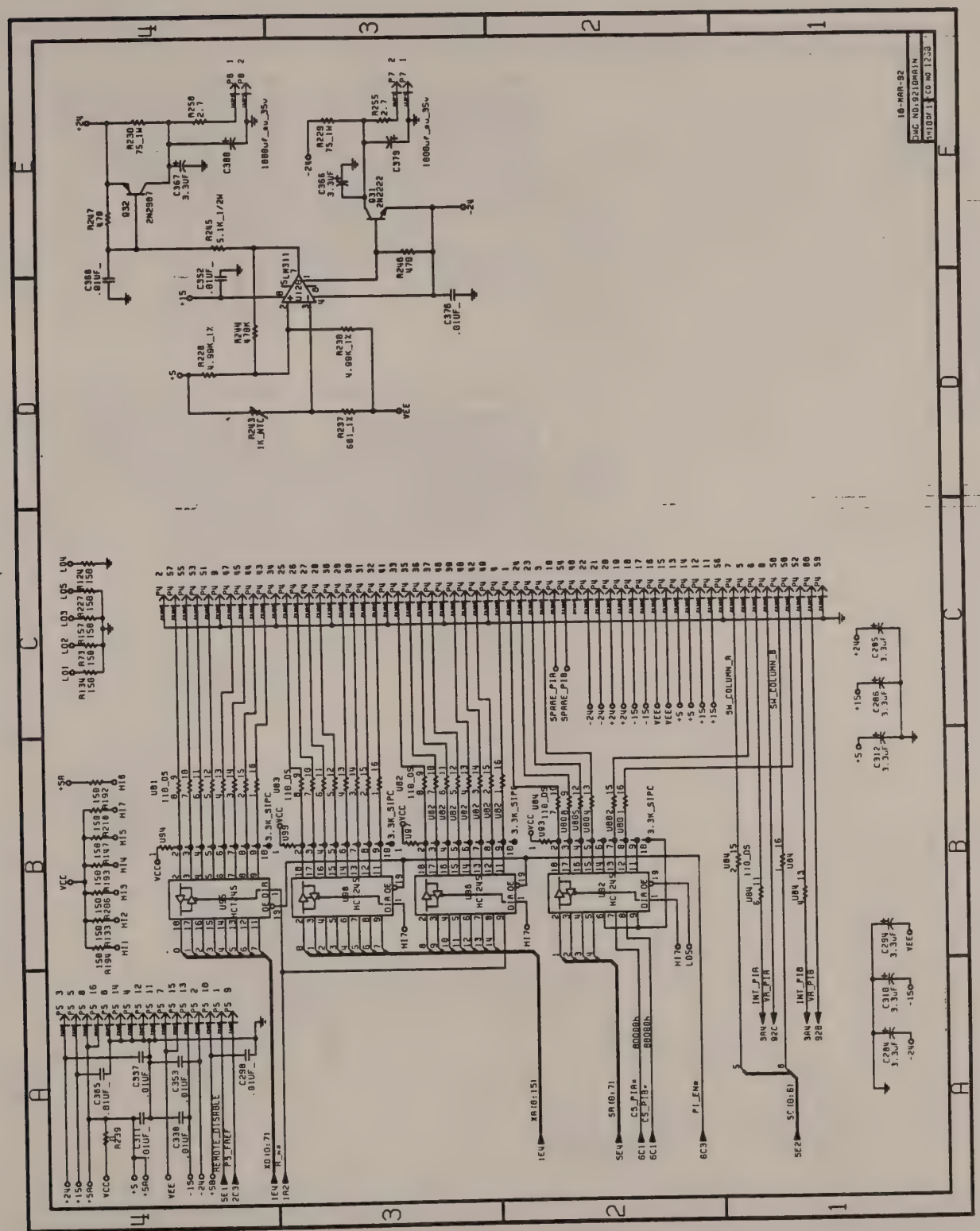
S7 9210 Main Schematics Rev B-7



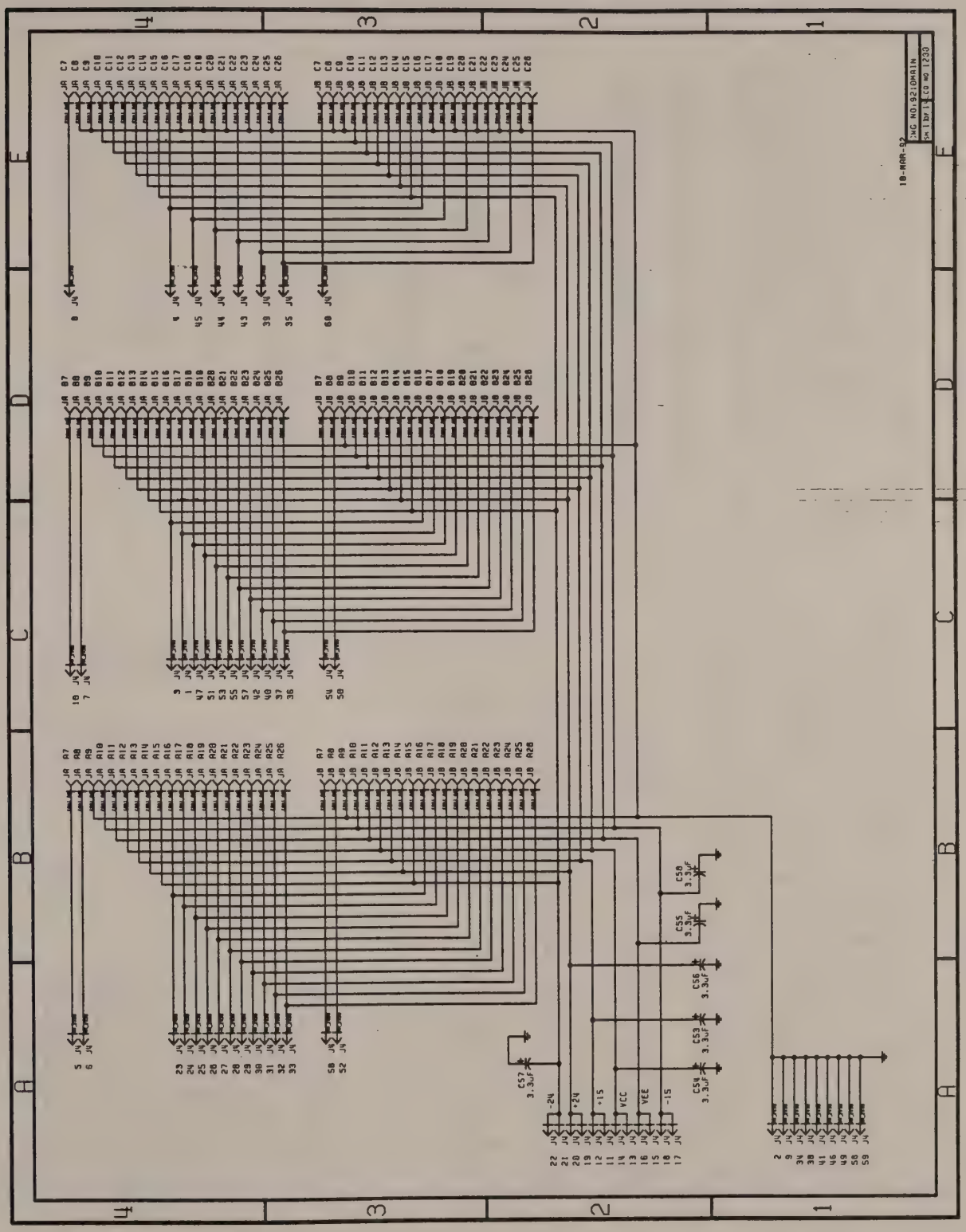
S8 9210 Main Schematics Rev B-8



S9 9210 Main Schematics Rev B-9

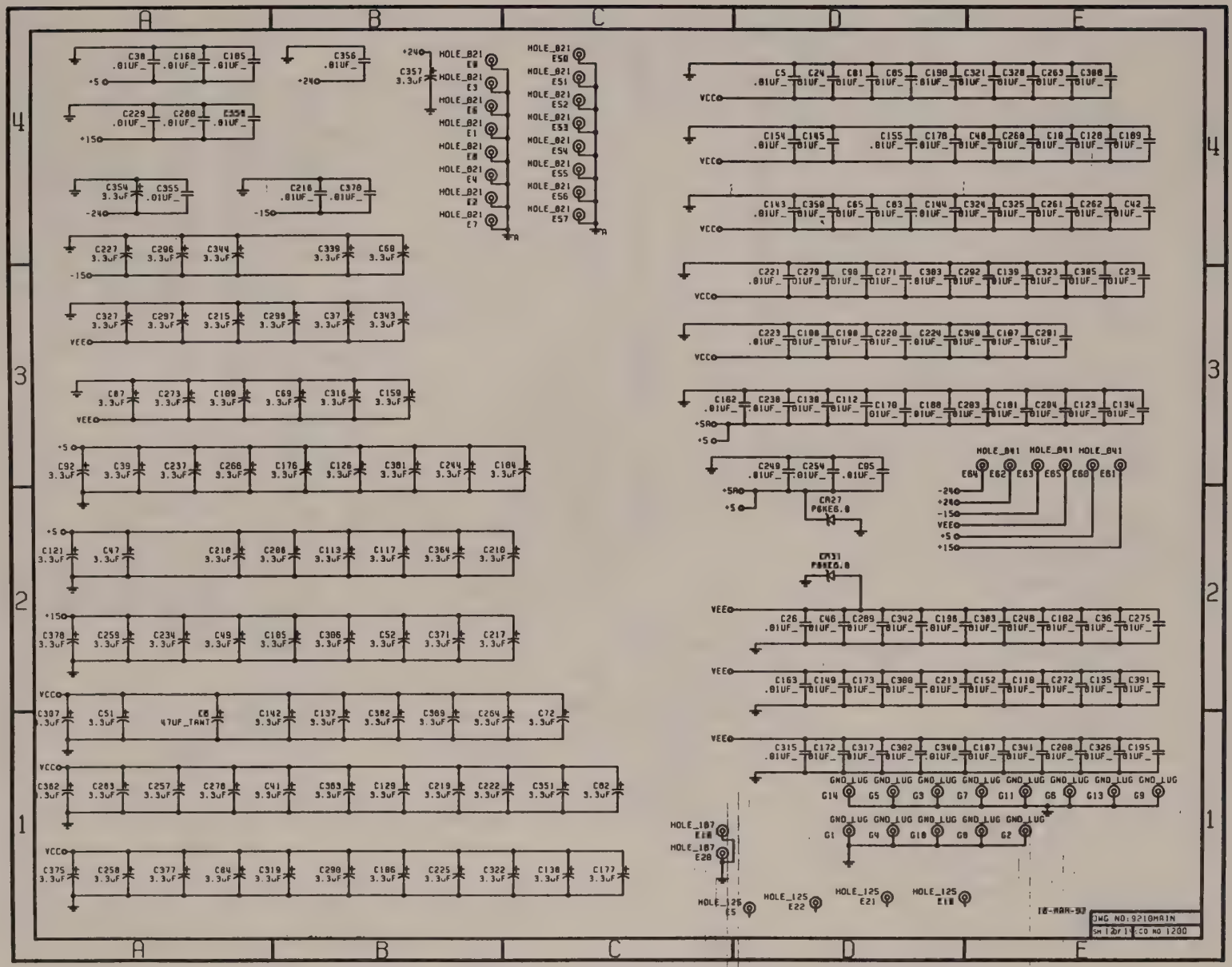


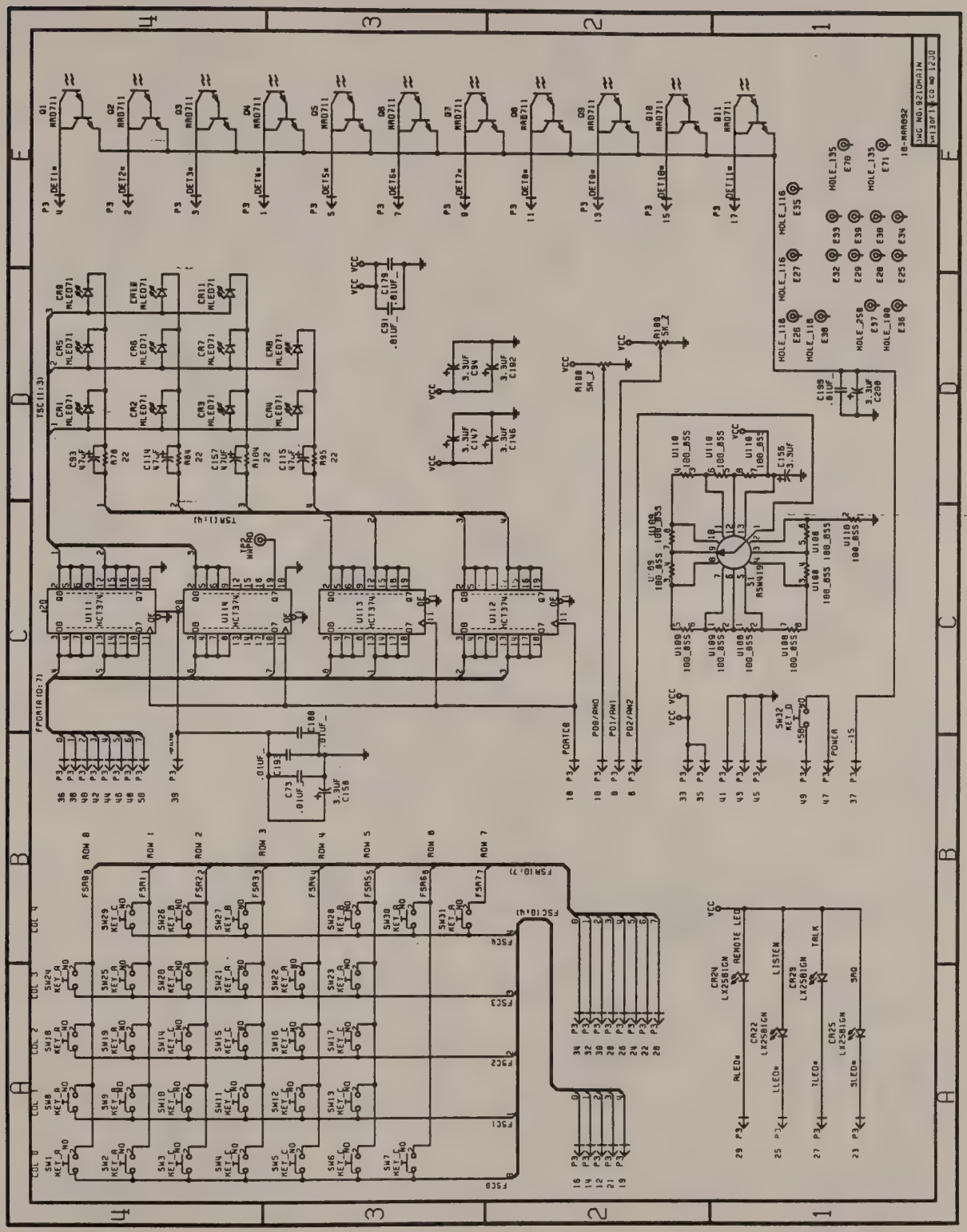
S10 9210 Main Schematics Rev B-10



S11 9210 Main Schematics Rev B-11

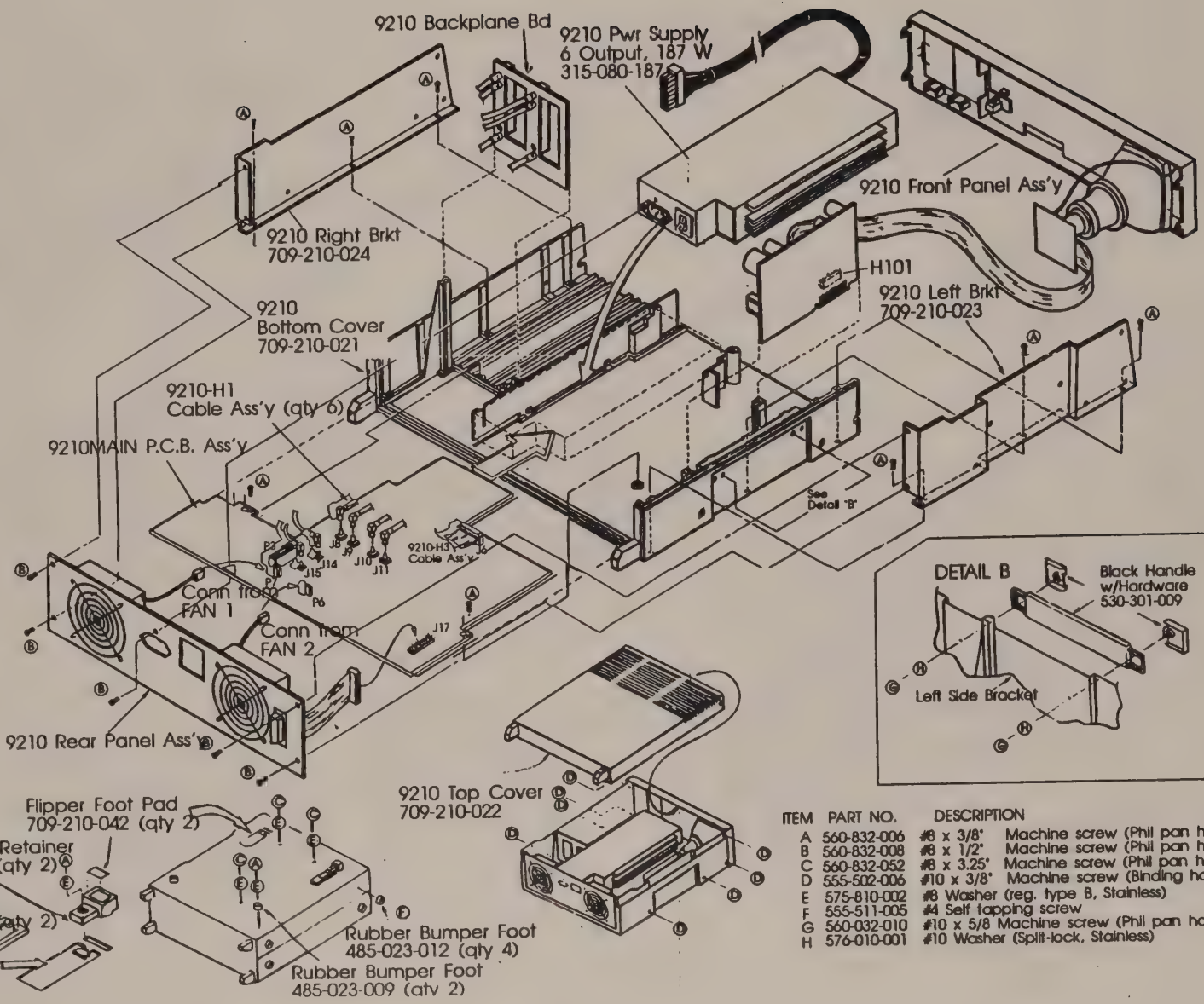
S12 9210 Main Schematics Rev B-12



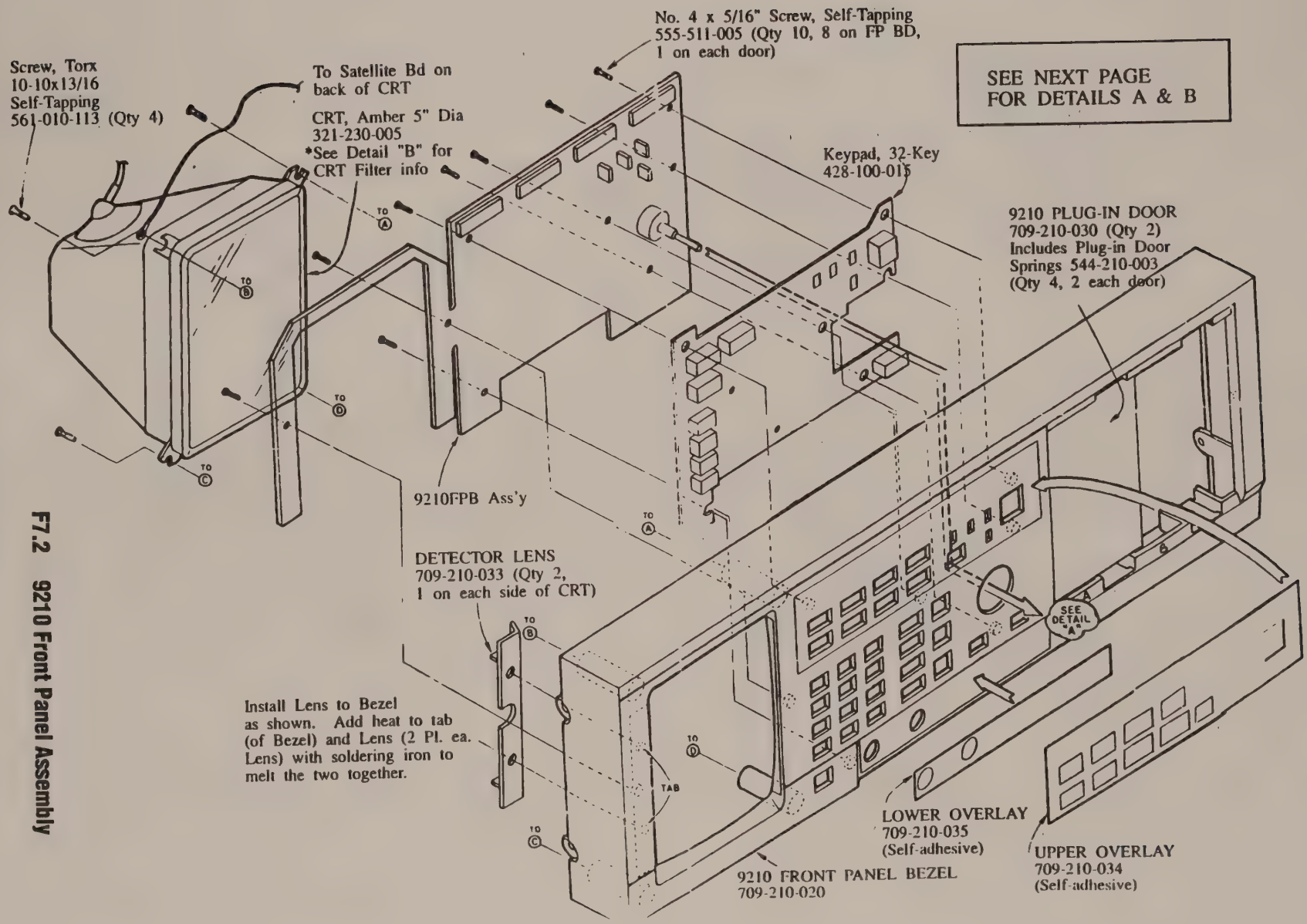


S13 9210 Main Schematics Rev B-13

F7.1 9210 Assembly

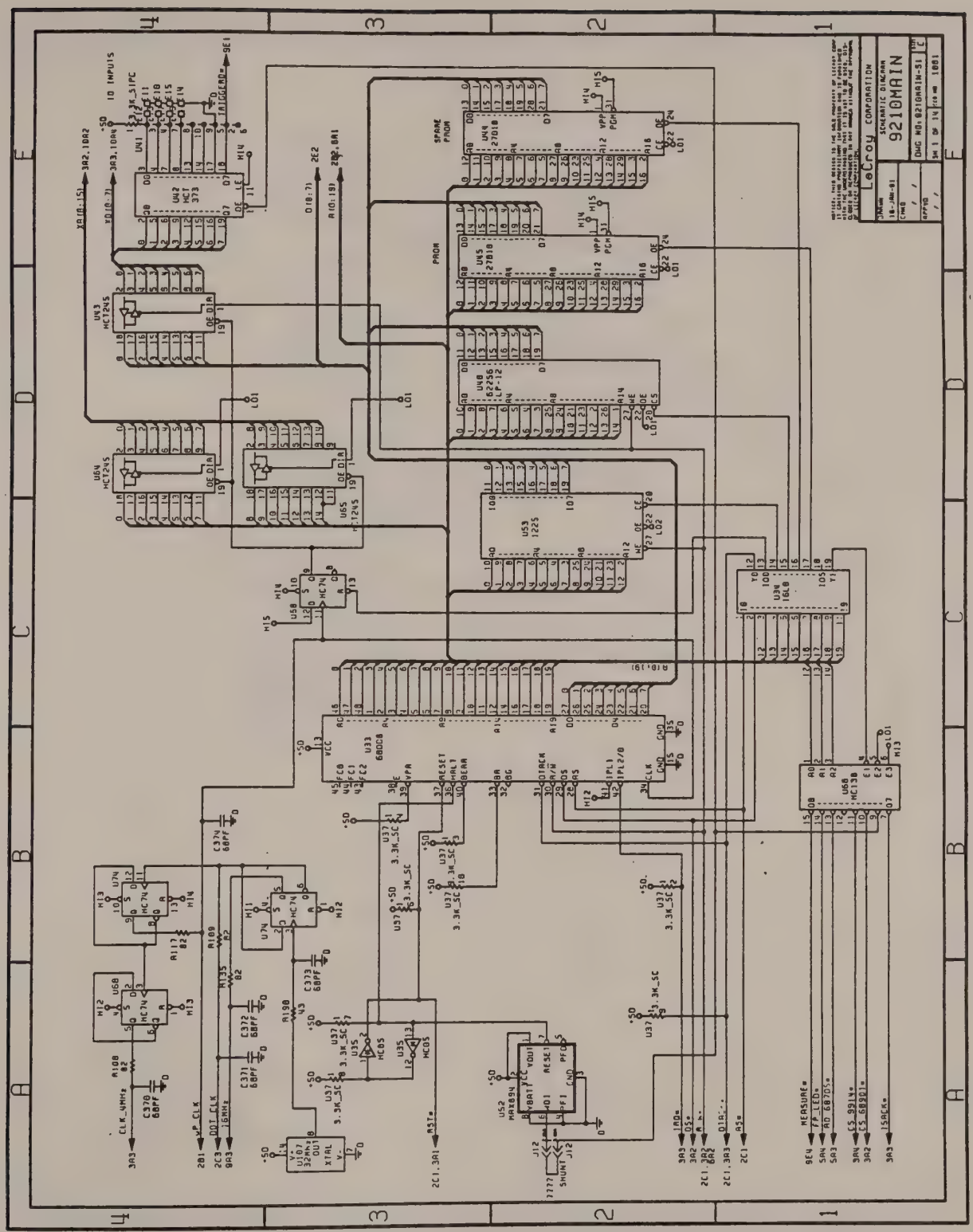


ITEM	PART NO.	DESCRIPTION	QTY
A	560-832-006	#8 x 3/8" Machine screw (Phil pan hd)	12
B	560-832-008	#8 x 1/2" Machine screw (Phil pan hd)	5
C	560-832-052	#8 x 3.25" Machine screw (Phil pan hd)	3
D	555-502-006	#10 x 3/8" Machine screw (Binding hd)	8
E	575-810-002	#8 Washer (reg. type B, Stainless)	7
F	555-511-005	#4 Self tapping screw	4
G	560-032-010	#10 x 5/8 Machine screw (Phil pan hd)	2
H	576-010-001	#10 Washer (Split-lock, Stainless)	2

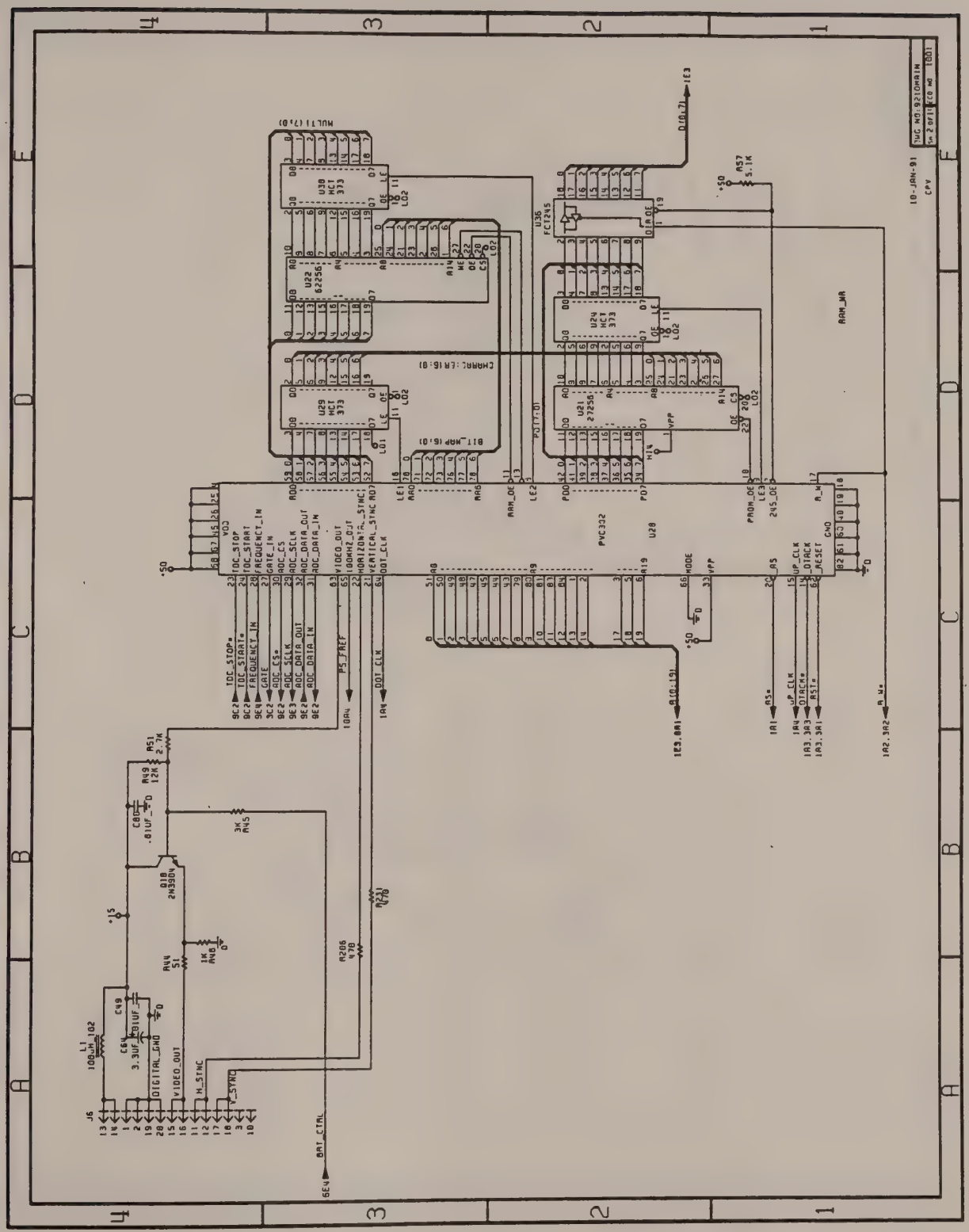


F7.2 9210 Front Panel Assembly

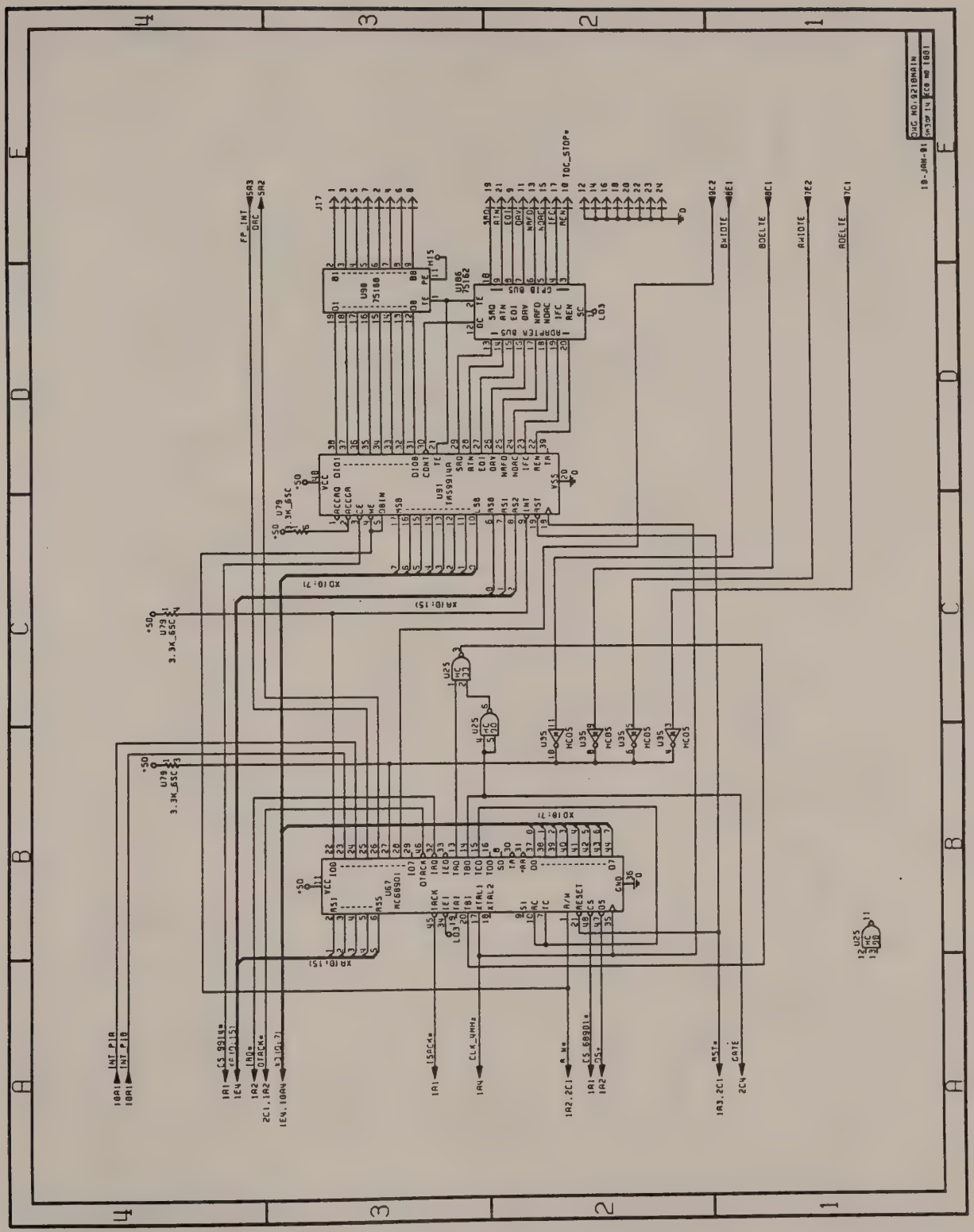
F7.3 Front Panel Details A&B



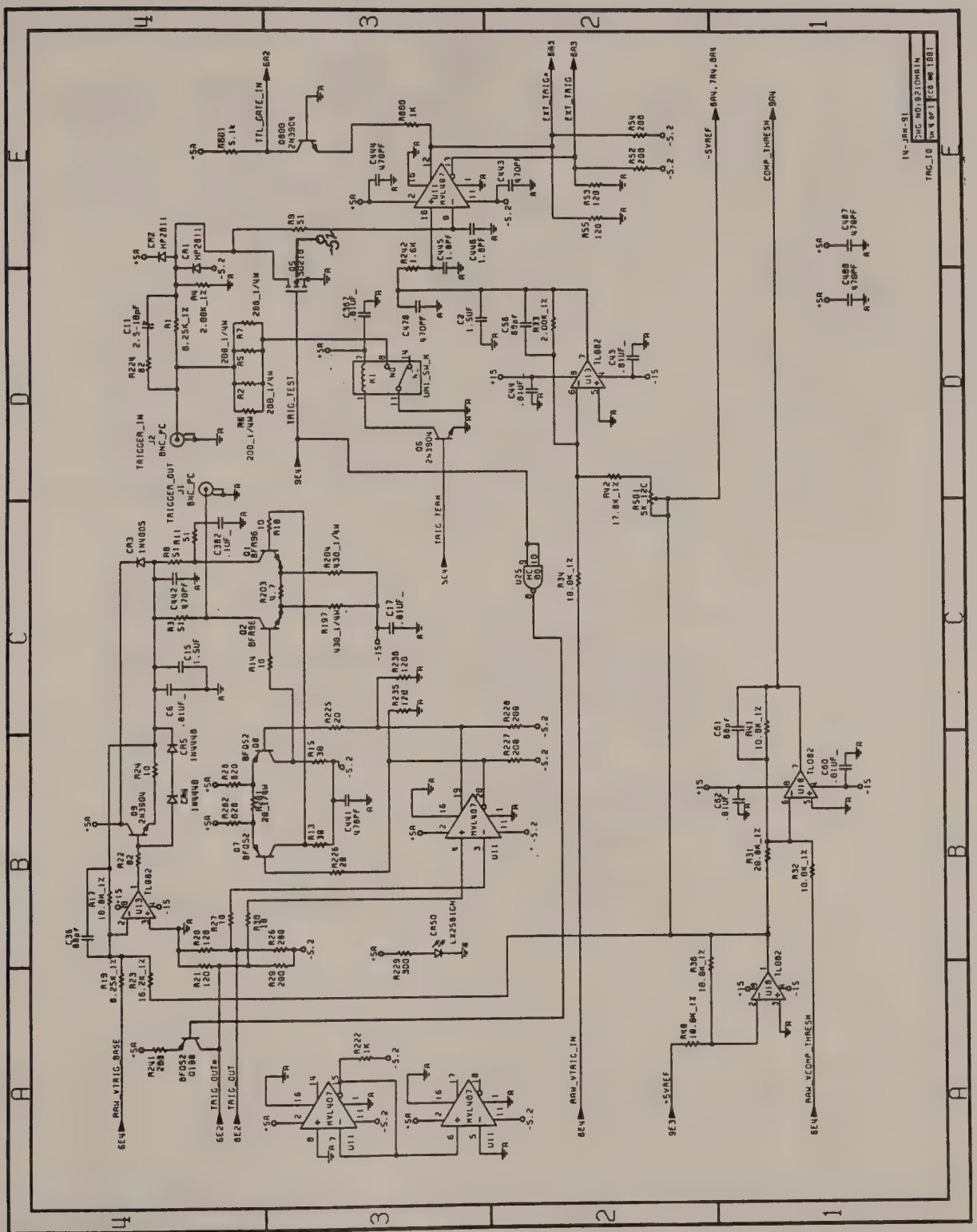
S15 9210 Main Schematics Rev A-1



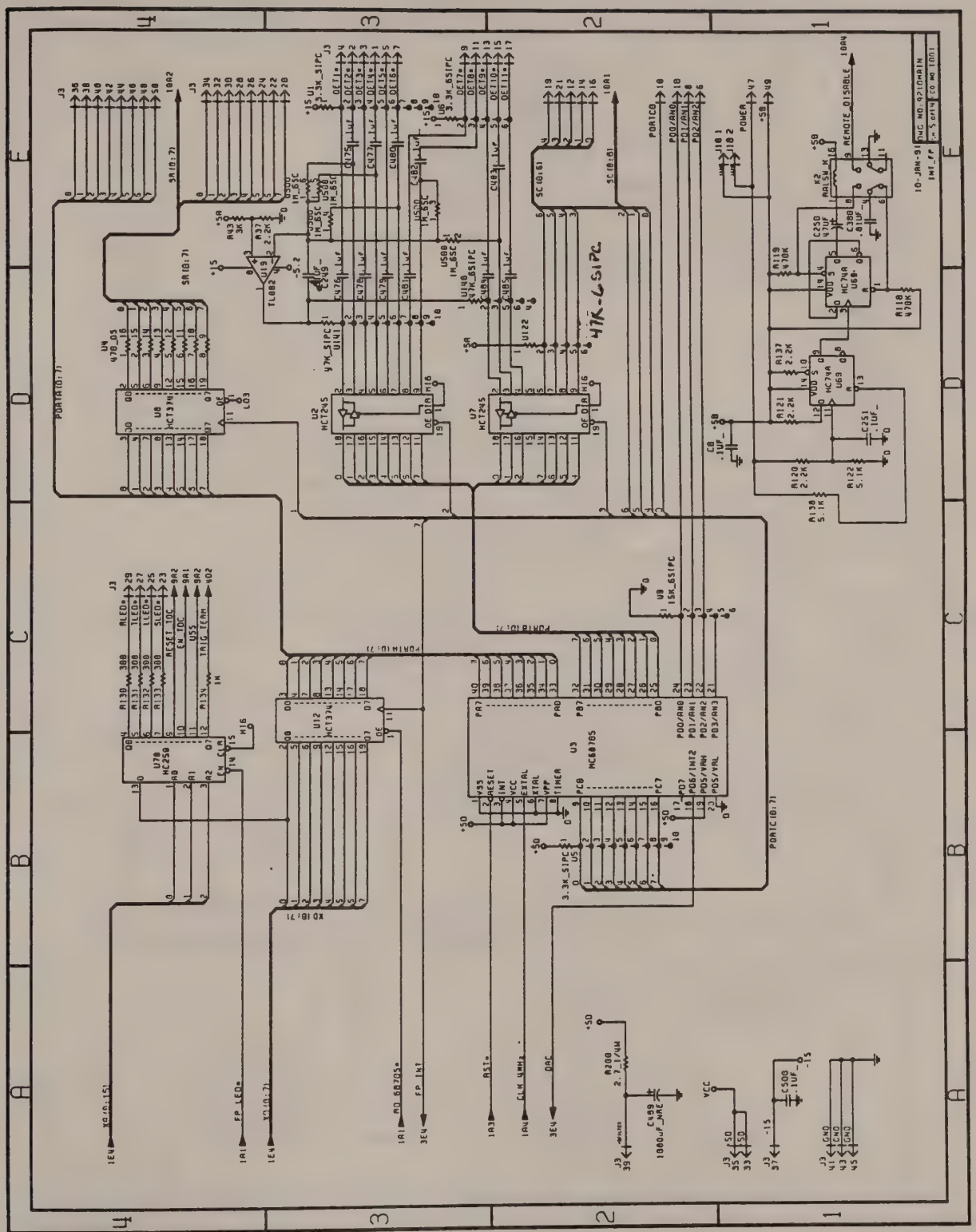
S16 9210 Main Schematics Rev A-2



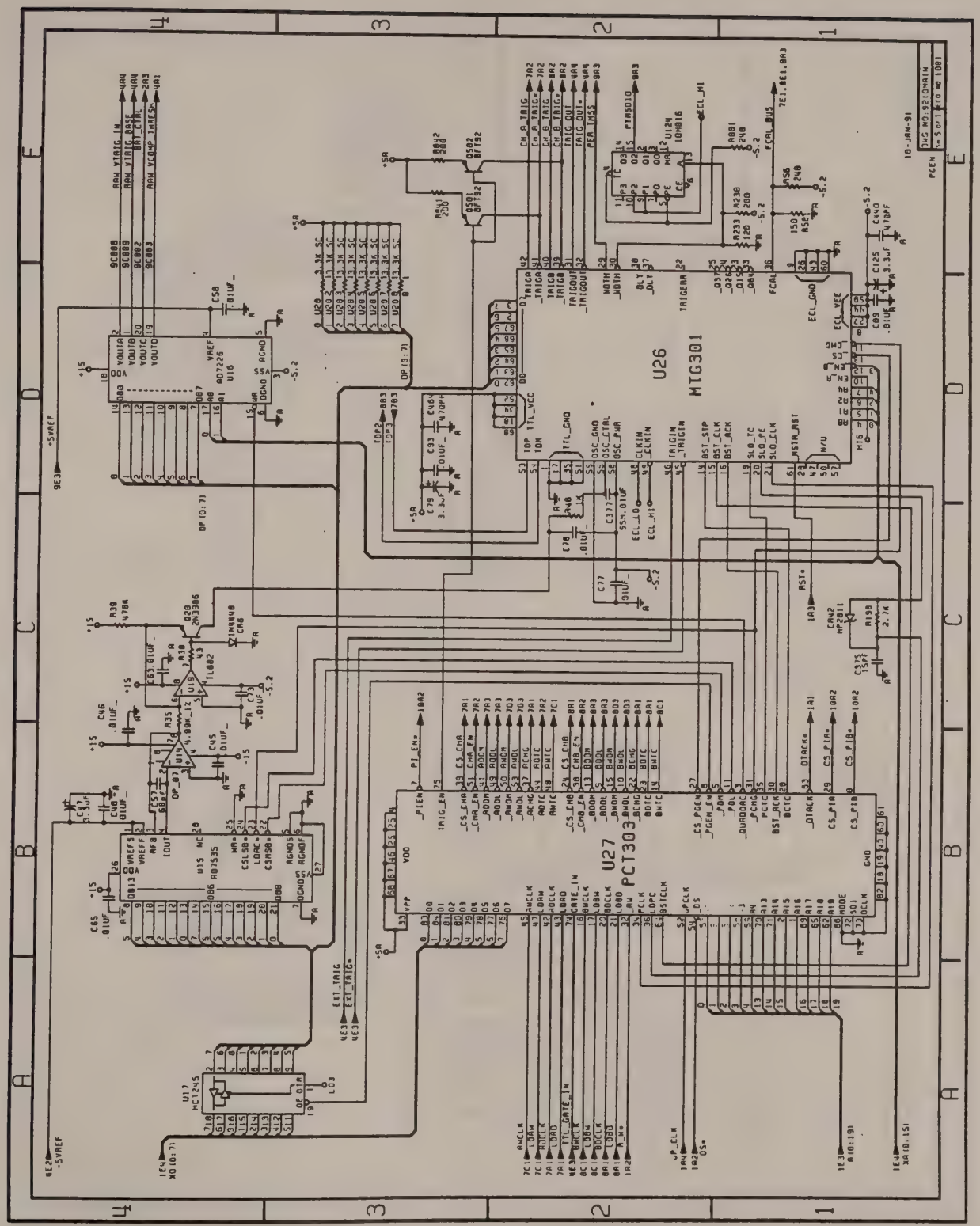
S17 9210 Main Schematics Rev A-3



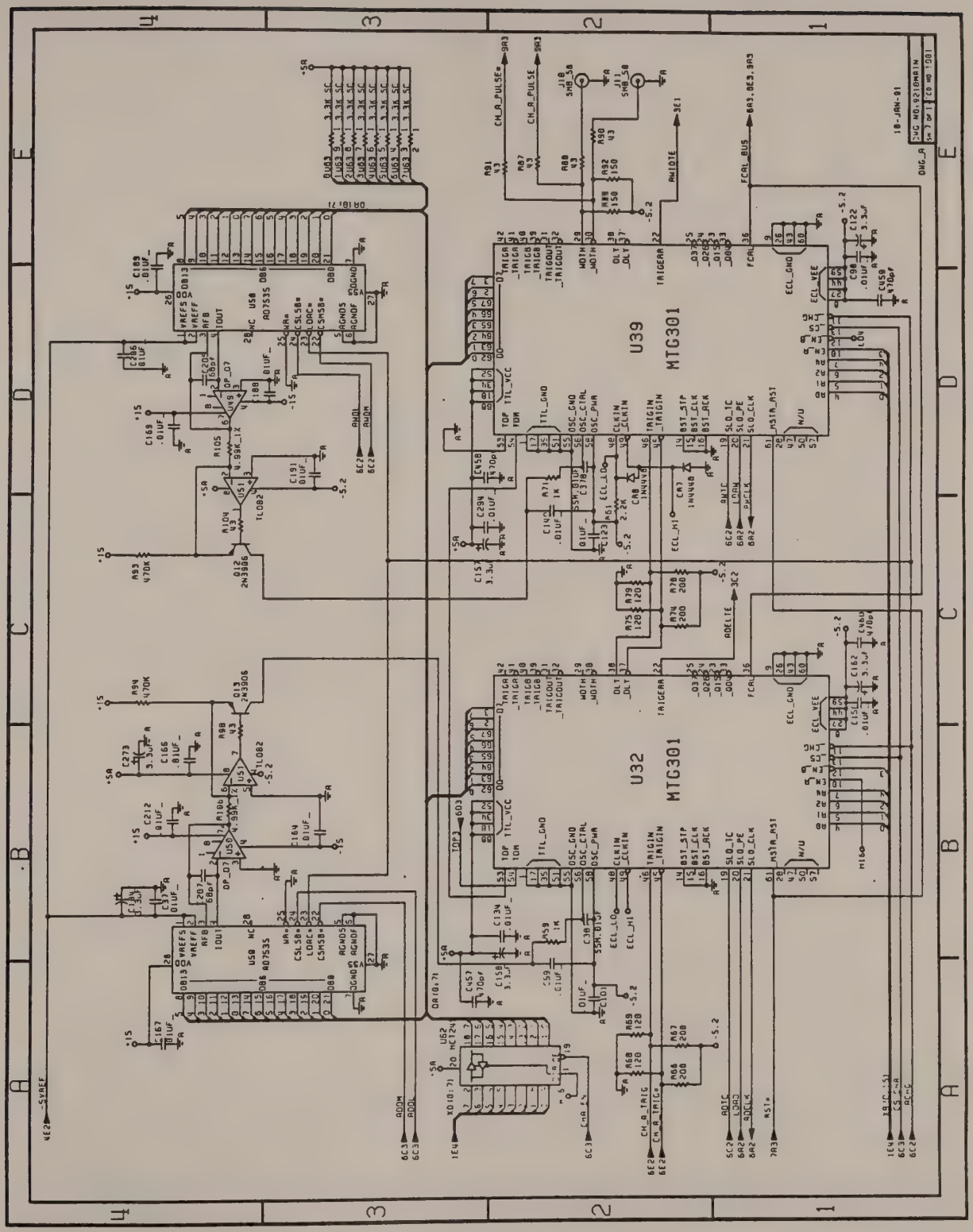
S18 9210 Main Schematics Rev A-4



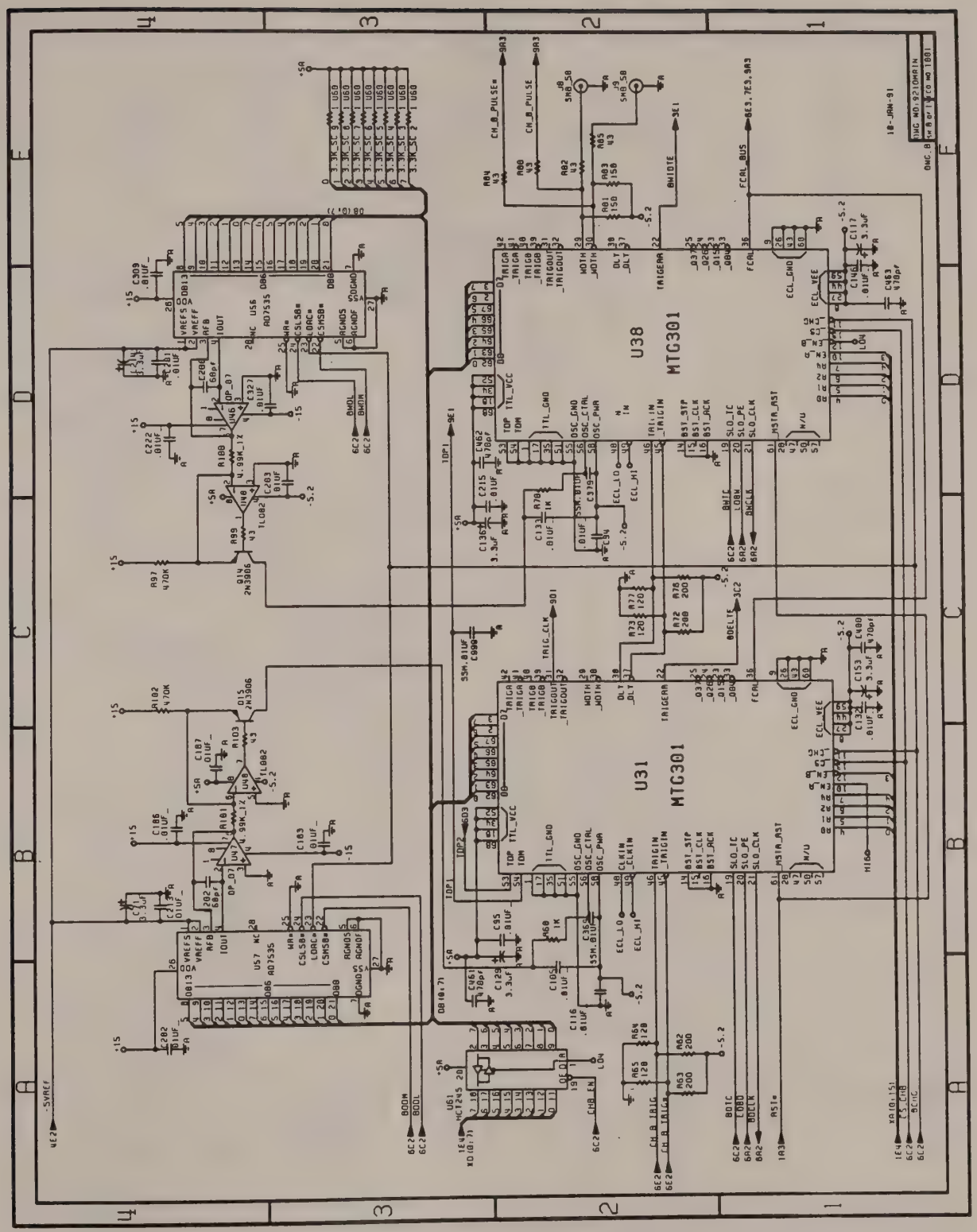
S19 9210 Main Schematics Rev A-5



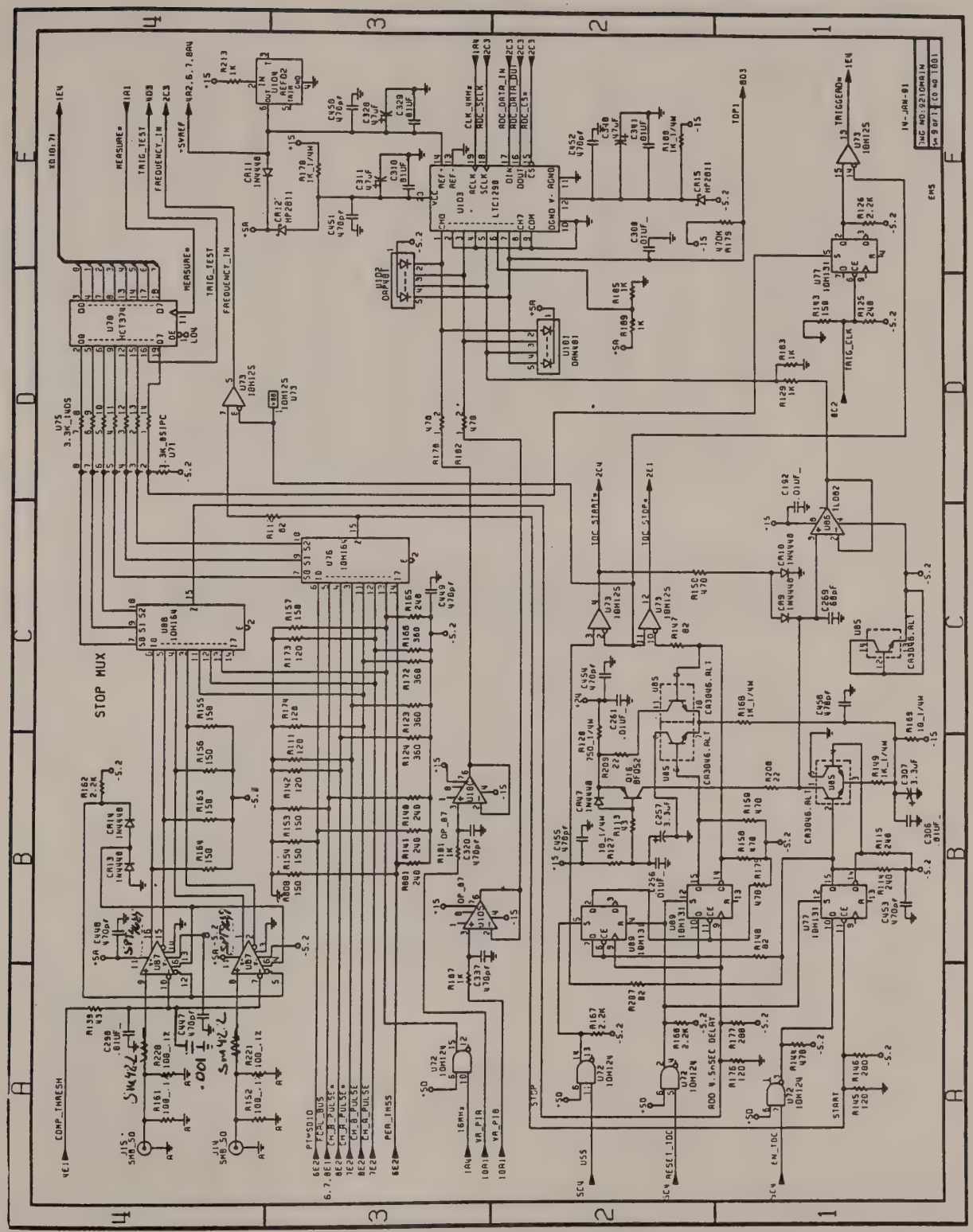
S20 9210 Main Schematics Rev A-6



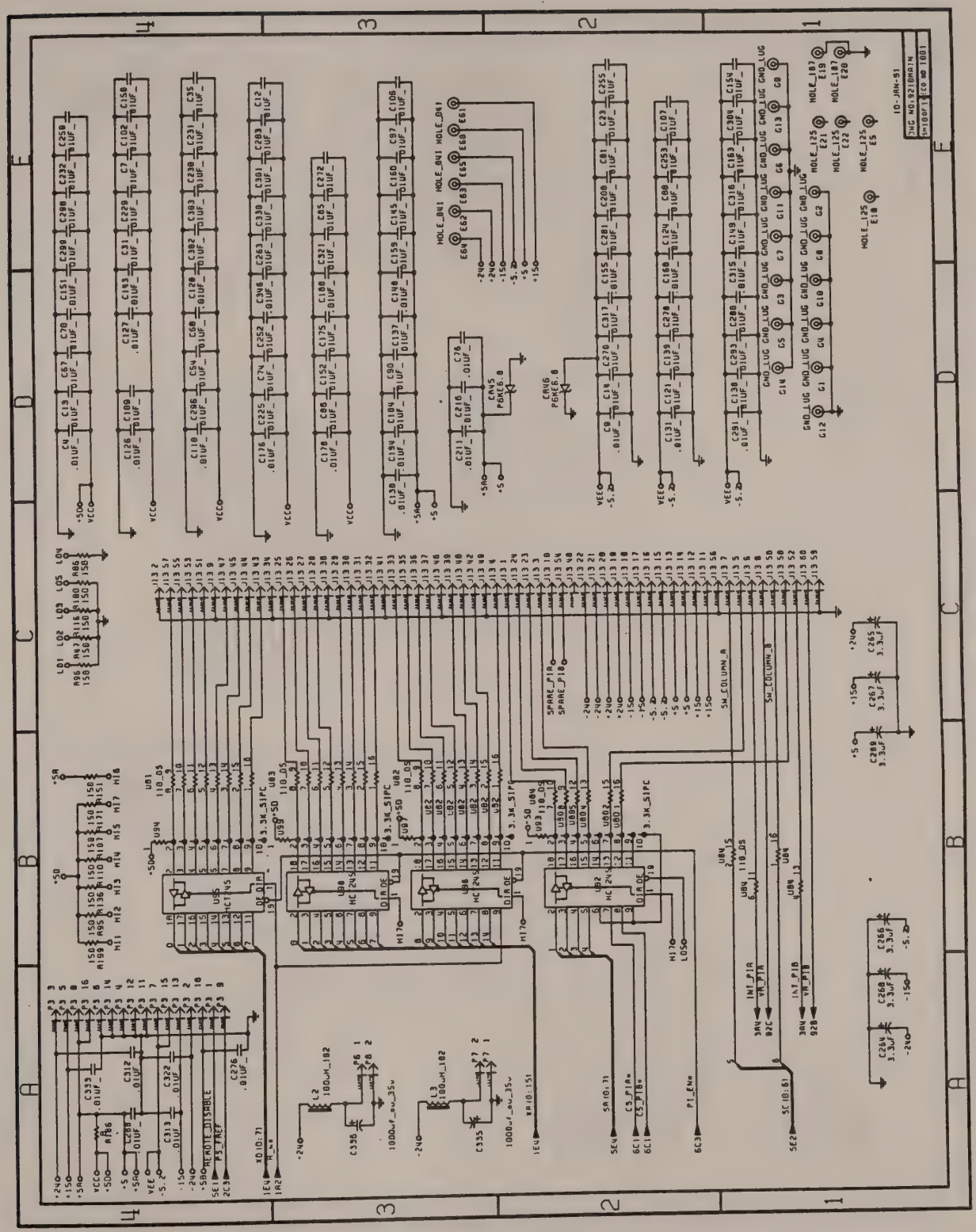
S21 9210 Main Schematics Rev A-7



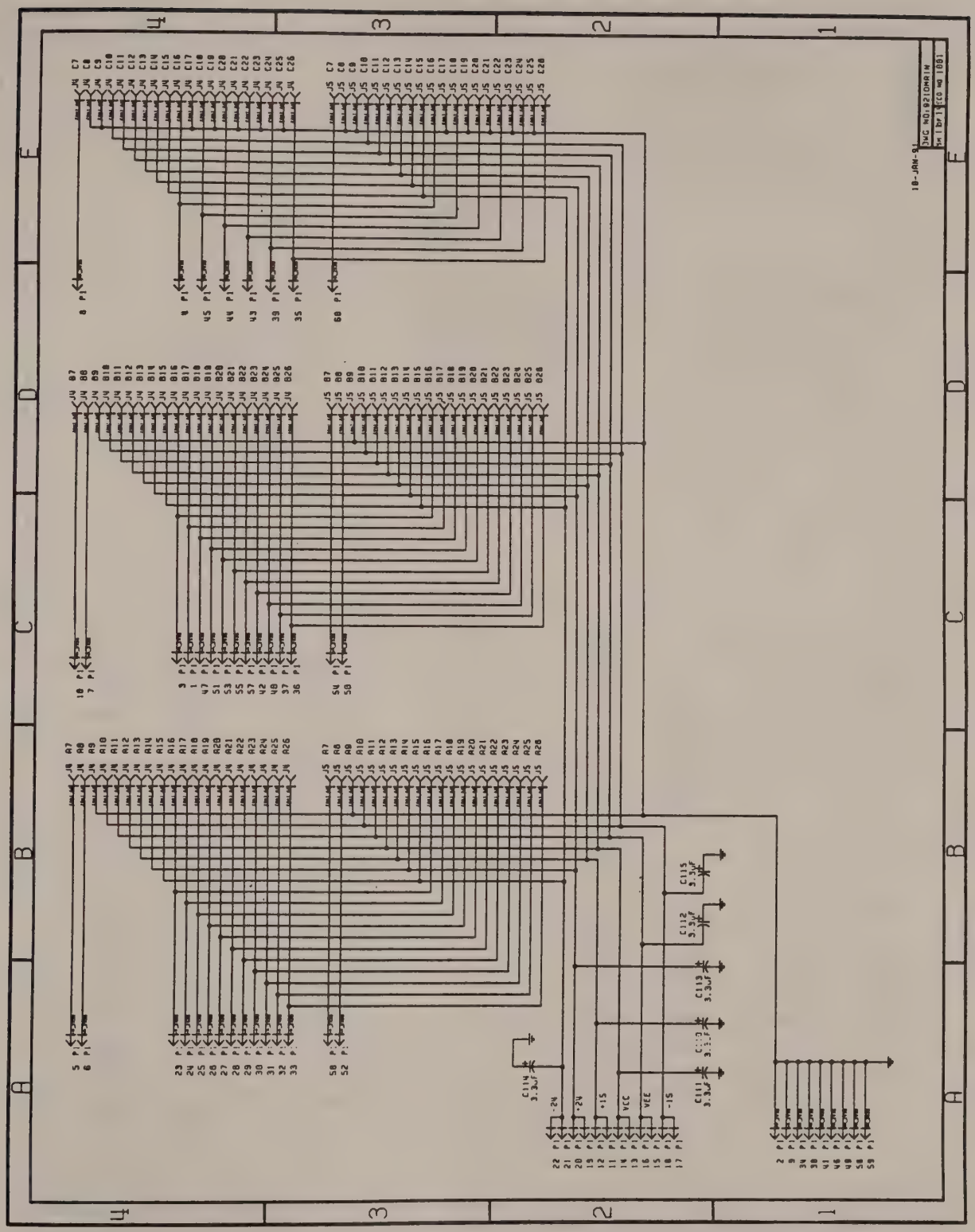
S22 9210 Main Schematics Rev A-8



S23 9210 Main Schematics Rev A-9

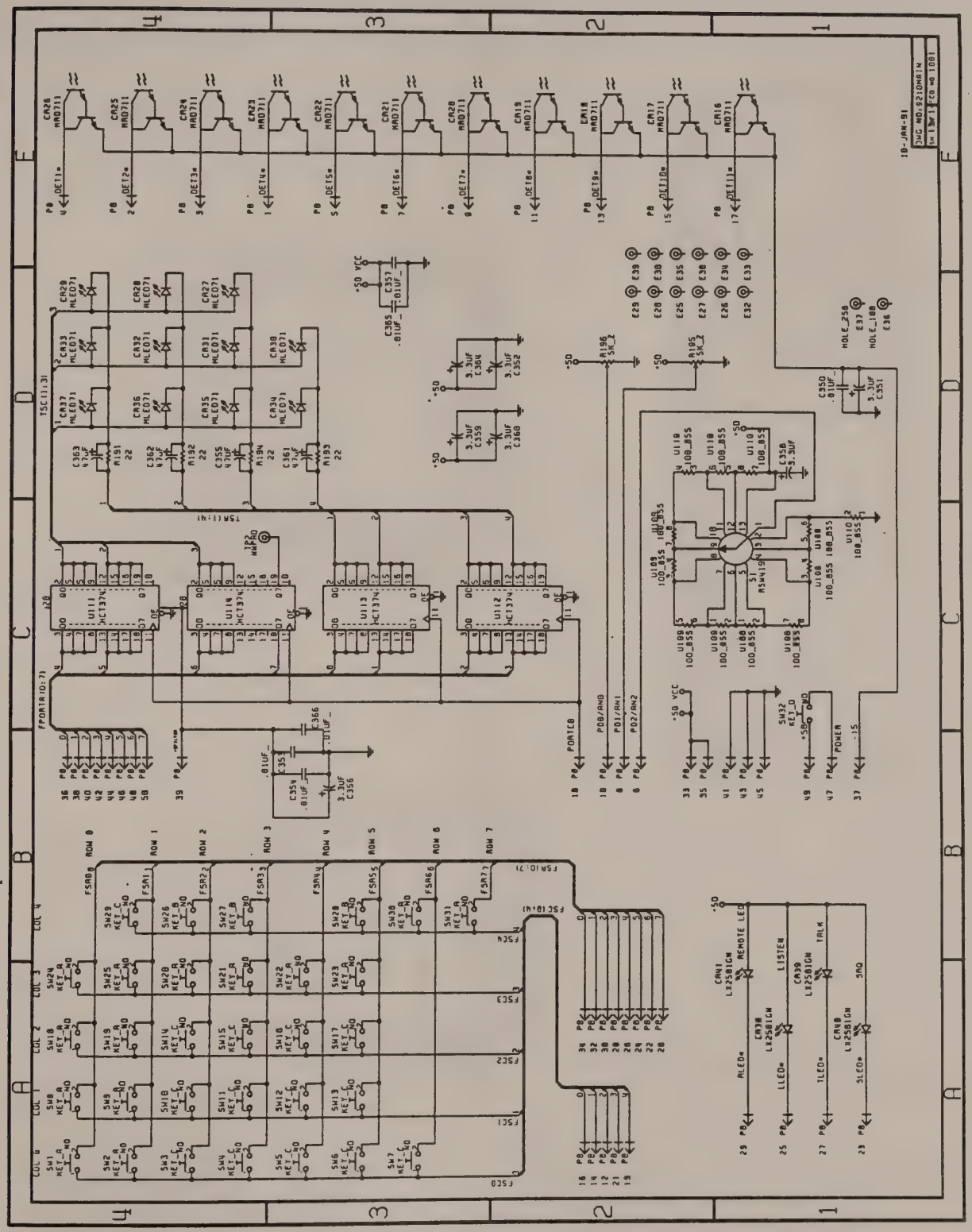


S24 9210 Main Schematics Rev A-10

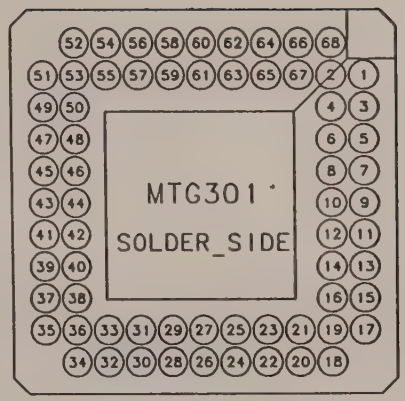


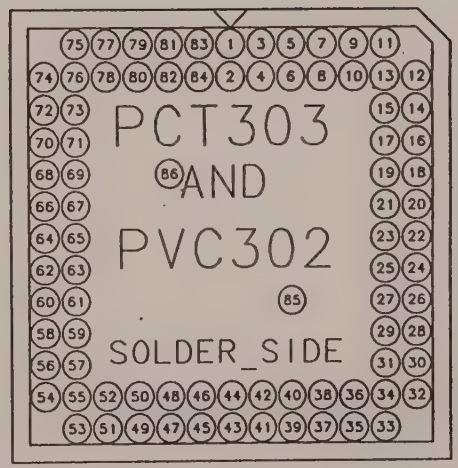
S25 9210 Main Schematics Rev A-11

S26 9210 Main Schematics Rev A-12



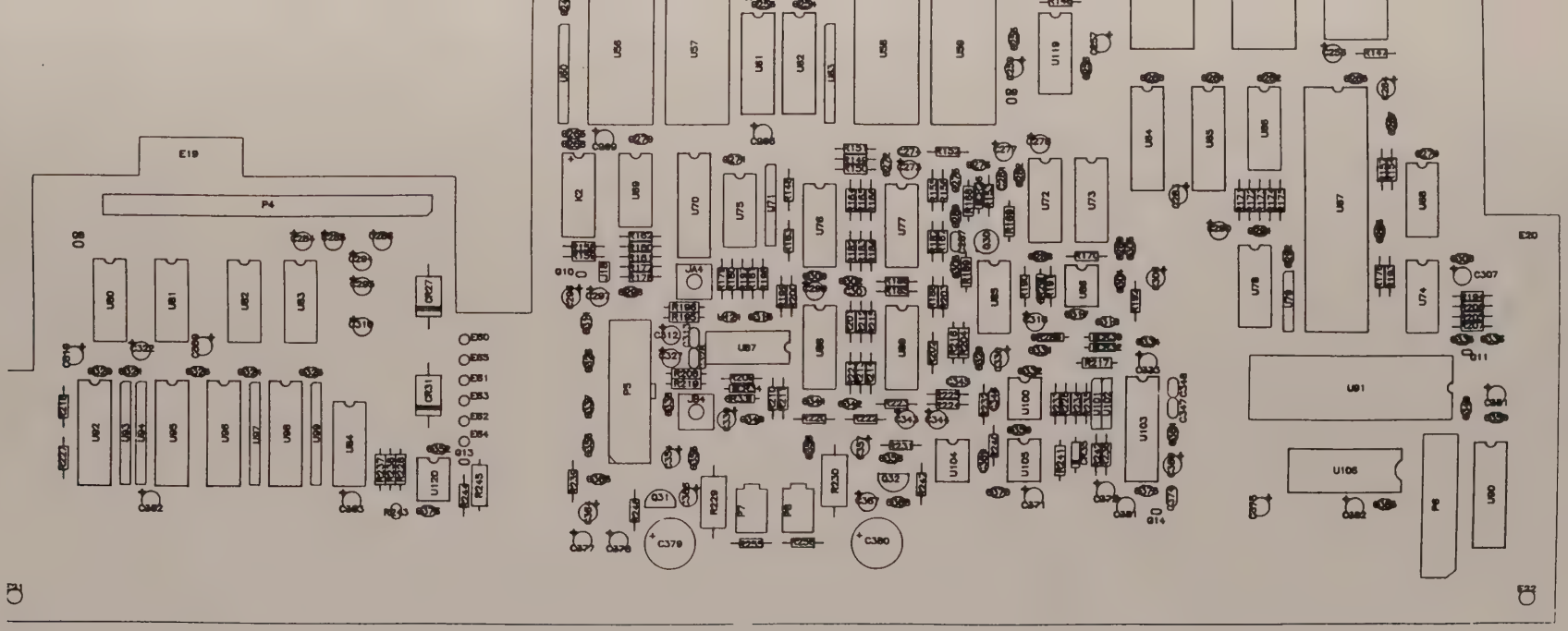
S27 9210 Main Schematics Rev A-13

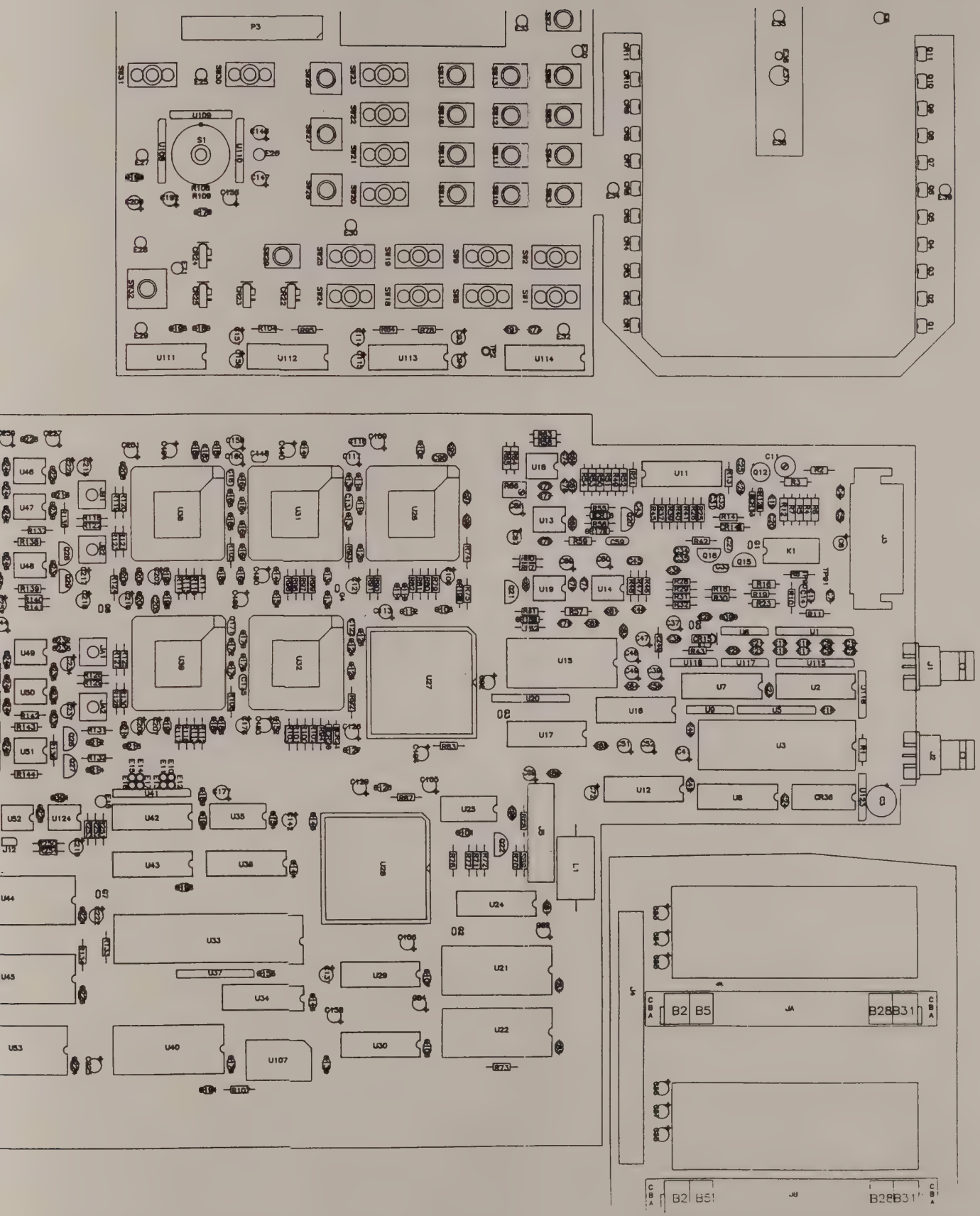




NOTICE: THIS DESIGN IS THE SOLE PROPERTY OF LeCROY RESEARCH SYSTEMS. IT CONTAINS PROPRIETARY INFORMATION AND IS FURNISHED WITH THE UNDERSTANDING THAT IT IS NOT TO BE USED, DISCLOSED OR REPRODUCED IN ANY MANNER WITHOUT THE APPROVAL OF LeCROY RESEARCH SYSTEMS.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE IN DECIMALS: 2PL ±.01, 3PL ±.005 ANGLE ±0°-15' ☐ DO NOT SCALE	LeCroy RESEARCH SYSTEMS	
	DRAWN BY/DATE J.B. 10/11/90	9210MAIN SCHEMATICS
	CHKD BY/DATE	
MATERIAL	APPROVED BY/DATE	DWG NO: 9210MAIN-S1 SIZE A
FINISH	SCALE NV	SH 14 OF 14 REV. ECO NO. 1001 DATE:


E19
P4
U50
U51
U52
U53
U54
U55
U56
U57
U58
U59
U60
U61
U62
U63
U64
U65
U66
U67
U68
U69
U70
U71
U72
U73
U74
U75
U76
U77
U78
U79
U80
U81
U82
U83
U84
U85
U86
U87
U88
U89
U90
U91
U92
U93
U94
U95
U96
U97
U98
U99
U100
U101
U102
U103
U104
U105
U106
U119
U120
P1
P2
P3
P5
P6
P7
P8
K2
JA4
C307
C379
C380
E20



S29 9210 Main Assembly Drawing

8.0 9210 Parts List

	COMPONENT #	DESCRIPTION REMARKS	QTY
1001			
	315080187	POWER SUPPLY 6 OUTPUT 187 W	1
	321230005	CRT AMBER 5" DIAGONAL	1
	323210005	CRT FILTER CONTOURED 5" DIAGONAL	1
	405747004	TERMINAL CRIMPED WIRE END	2
	428100015	KEPAD 32-KEY ELASTOMERIC	1
	453910003	CONN HDW KIT METRIC	1
	454120002	HDR SOLD TAIL/FEM 2	2
	455021015	CONTACT (CRIMP) FEMALE	4
	485023009	BUMPER (FOOT) BLACK RUBBER	2
	485023012	BUMPER (FOOT) BLACK RUBBER	4
	510090000	GOUNDING CLIP/BLADE	1
	530301009	BLK HANDLE W/2 BLK END CAPS	1
	530409036	FINGER GUARD FOR GLOBE MOTORS FAN	2
	530409137	FAN TUBEAXIAL 3.6" SQ X 1"	2
	542100001	OUTER KNOB COLLET 9210	1
	542100002	OUTER KNOB SLEEVE 9210	1
	542100003	OUTER KNOB WASHER 9210	1
	542100004	OUTER KNOB NUT 9210	1
	542200001	INNER KNOB COLLET 9210	1
	542200002	INNER KNOB SLEEVE 9210	1
	542200003	INNER KNOB WASHER 9210	1
	542200004	INNER KNOB SCREW 9210	1
	544210003	SPRING PLUG-IN DOOR RIGHT	4
	555502006	SCREW BINDING DN 10-32X3/8	8
	555511005	SCREW SELF-TAPPING PHIL HD	14
	560032010	SCREW PHILIPS 10-32X5/8	2
	560832006	SCREW PHILIPS 8-32X3/8	12
	560832008	SCREW PHILIPS 8-32X1/2	9
	560832052	SCREW PHILIPS 8-32 X 3.25"	3
	561010113	SCREW TORX 10-10X13/16	12
	575810002	WASHER FLAT REG OD SIZE 8	7
	576010001	WASHER SPLIT LOCK SIZE 10	4
	580632001	NUT HEX 6-32	1
	589203318	AC PWR CORD 3-COND	1
	590001018	WIRE TEFLON 19/30 BLK 18	1
	597921001	SHIPPING CARTON 9210	1
	597921003	SHIPPING CARTON TOP CAP 9210	1
	597921004	SHIPPING CARTON BOT CAP 9210	1
	709210020	9210 BEZEL	1
	709210021	BOTTOM COVER	1
	709210022	9210 TOP COVER	1
	709210023	9210 LEFT BRACKET	1
	709210024	9210 RIGHT BRACKET	1
	709210025	9210 REAR PANEL	1
	709210030	9210 PLUG-IN DOOR	2
	709210031	9210 FLIPPER FOOT	2
	709210032	9210 FLIPPER FOOT RETAINER	2
	709210033	DETECTOR LENS	2
	709210034	UPPER OVERLAY TRIM	1
	709210035	LOWER OVERLAY TRIM	1
	709210037	3 PIECE CONCENTRIC KNOB SET 9210	1
	709210042	9210 FRONT FOOT PAD	2
	709210050	CLAMPING BRACKET LEFT SIDE	1
	709210051	CLAMPING BRACKET RIGHT SIDE	1
	9210-H1	CABLE CO-AX 10" SMB-PHOENIX PLUG	6
	9210-H2	RIBBON CABLE 4.5" 24 COND	1
	9210-H3	RIBBON CABLE 9" 20 COND	1
	9210/OM	9210 OPERATOR'S MANUAL	1
	9210MAIN	9210 MAIN BOARD	1

8.1 9210 Main Parts List

COMPONENT #	DESCRIPTION REMARKS	QTY
1112		
102412018	CAP CERA DISC 100V 1.8 PF C31,C32	2
102412022	CAP CERA DISC 100V 2.2 PF	1
102484471	CAP CERA DISC 100V 470 PF C20,C25,C27,C33-C35, C43,C45,C96,C116, C122,C131,C148,C161, C171,C175,C182,C205, C274,C281,C287,C301, C313,C328,C345-C348, C369,C374	30
103347155	CAP CERA MONO 50V 1.5 UF C14,C59	2
106423270	CAP CERA MONO 27PF C120	1
106425103	CAP CERA MONO .01UF C5,C10,C13,C19,C23, C24,C26,C28,C36,C38, C40,C42,C46,C50,C61, C63-C66,C68,C71 C73,C74,C76,C77,C79- C81,C83,C85,C88,C90, C91,C95,C97,C99,C101 C102,C107,C108,C110- C112,C118,C119,C123- C125,C127,C128,C130, C133-C135,C139,C141, C143-C145,C149,C151, C152,C154,C155,C162- C168,C170,C172-C174, C178-C181,C183,C185, C187-C190,C193,C195- C199,C203,C204,C208, C209,C211-C214,C216, C221,C221,C223,C224, C226,C229-C233,C235, C236,C238,C241,C243, C246,C248-C251,C253- C256,C260-C263,C265, C268,C271,C272,C275, C276,C279,C280,C282, C289,C291,C292,C298, C300,C302-C305,C308, C311,C314,C315,C317, C318,C320,C321,C323- C326,C329,C331,C332, C334,C337,C338,C340- C342,C349,C350,C352, C353,C355,C356,C358, C359,C361,C365,C368, C370,C373,C376,C383	182
106428104	CAP CERA MONO .1UF C1,C2,C4,C7-C9,C15- C18,C21,C22,C29,C270 C70	15
106443150X	CAP CERA MONO 15PF C375	1
106443680X	CAP CERA MONO 68PF C62,C67,C75,C78,C191	14

	COMPONENT #	DESCRIPTION REMARKS	QTY
1112			
		C240,C242,C245,C247, C267,C288,C293,C335, C336	
	141268476	CAP TANT DIP CASE 10V 47UF C6,C93,C114,C115, C157,C269,C233,C360, C372	9
	141838335	CAP TANT DIP REEL 3.3UF C37,C39,C41,C47-C49, C51-C58,C60,C69,C72, C82,C84,C86,C87,C89, C92,C94,C100,C104, C105,C106,C109,C113, C117,C121,C126,C129, C137,C138,C140,C142, C146,C147,C150,C153, C156,C158-C160,C169, C176,C177,C192,C194, C200-C202,C206,C207, C210,C215,C217-C219, C222,C225,C227,C228, C234,C237,C239,C244. C252,C257-C259,C264, C266,C273,C277,C278, C283-C286,C290,C294- C297,C209,C306,C307, C309,C310,C312,C316, C319,C322,C327,C330, C339,C343,C344,C351, C354,C357,C362-C364, C366,C367,C371,C375, C377,C378,C381,C382	115
	146164108	CAP MINI ALUM 20% 1000 UF C3	1
	146644108	CAP MINI ALUM 20% 1000 UF C379,C380	2
	158879003	CAP VARIABLE 2.5-10 PF C11	1
	161030000	RES COMP ZERO OHMS R19,R239	2
	161225100	RES CARBON FILM 10 OHMS R40,R41,R56	3
	161225101	RES CARBON FILM 100 OHMS	1
	161225102	RES CARBON FILM 1 K R13,R72,R74,R92,R93, R105,R106,R170,R175, R231,R232,R234,R236, R240,R242	15
	161225121	RES CARBON FILM 120 OHMS R25,R37,R79,R81,R98, R99,R102,R103,R111, R113,R115,R117,R146, R148,R151,R182,R186, R221,R222,R225	20
	161225123	RES CARBON FILM 12 K R47,R77	2
	161225151	RES CARBON FILM 150 OHMS R28,R29,R31,R32,R73, R91,R120,R121,R124,	29

	COMPONENT #	DESCRIPTION REMARKS	QTY
1112		R125,R130,R133,R134, R147,R157,R183,R192, R193,R194,R197-R201, R206,R210,R211,R218, R227	
	161225162	RES CARBON FILM 1.6 K R42,R46	2
	161225201	RES CARBON FILM 200 OHMS R26,R39,R45,R80,R82, R96,R97,R100,R101, R110,R112,R114,R116, R145,R149,R185,R224	17
	161225202	RES CARBON FILM 2 K R48	1
	161225220	RES CARBON FILM 22 OHMS R78,R84,R95,R104, R167,R190	6
	161225222	RES CARBON FILM 2.2 K R60,R94,R160,R161, R166,R178,R209,R214, R215	9
	161225241	RES CARBON FILM 240 OHMS R90,R155,R156,R165, R180,R181,R212	7
	161225272	RES CARBON FILM 2.7 K R75,R76	2
	161225301	RES CARBON FILM 300 OHMS R43,R171-R174	5
	161225302	RES CARBON FILM 3 K R67,R71	2
	161225361	RES CARBON FILM 360 OHMS R163,R164,R213,R220	4
	161225430	RES CARBON FILM 43 OHMS R61,R107,R118,R119, R122,R123,R126-R129, R136,R137,R141,R142, R153,R179	16
	161225471	RES CARBON FILM 470 OHMS R68,R69,R184,R191, R202,R203,R223,R226, R233,R246,R247	11
	161225474	RES CARBON FILM 470 K R62,R131,R132,R135, R140,R158,R159,R235, R244	9
	161225510	RES CARBON FILM 51 OHMS R8,R10,R11,R14,R70	5
	161225512	RES CARBON FILM 5.1 K R83,R87,R162,R167	4
	161225621	RES CARBON FILM 620 OHMS R18,R21	2
	161225820	RES CARBON FILM 82 OHMS R2,R55,R150,R152, R154,R176,R187,R188, R205,R207	10
	161335027	RES CARBON FILM 2.7 OHMS R1	1
	161335100	RES CARBON FILM 10 OHMS R168,R216	2

9210 Main Parts List

COMPONENT #	DESCRIPTION REMARKS	QTY
1112		
161335102	RES CARBON FILM 1 K R189,R204,R217,R241	4
161335201	RES CARBON FILM 200 OHMS R4-R7	4
161335431	RES CARBON FILM 430 OHMS R16,R23	2
161335751	RES CARBON FILM 750 OHMS R11,R128 R169	1
161445512	RES CARBON FILM 5.1 K R245	1
161555750	RES COMP 1W 5% 75 OHMS R229,R230	2
168139297	RES RN55E .1% 100 OHMS R195,R196,R208,R219	4
168139489	RES RN55E .1% 10 K R54,R58,R63,R64	4
168139518	RES RN55E .1% 20.0 K R65	1
168531377	RES PREC RN55D 681 OHMS R237	1
168531422	RES PREC RN55D 2.00 K R12,R159	2
168531460	RES PREC RN55D 4.99 K R57,R138,R139,R143, R144,R238,R338	7
168531481	RES PREC RN55D 8.25 K R3,R52	2
168531489	RES PREC RN55D 10.0 K R49,R53	2
168531509	RES PREC RN55D 16.2 K R51	1
168531513	RES PREC RN55D 17.8 K R50	1
180247502	RES VARI CERMET 5 K R66	1
184547502	RES VARI COND PLASTIC 5K R108,R109 GIVE TO SSD MANUF.	1
190042332	RESISTOR NETWORK 3.3 K U1,U20,U37,U41, U60,U63,U93,U94,U97, U99	10
190042473	RESISTOR NETWORK 47 K U115,U5	2
190322332	RESISTOR NETWORK 3.3 K U75	1
190332111	RESISTOR NETWORK 110 OHMS U80-U84	5
190332471	RESISTOR NETWORK 470 OHMS U4	1
190642105	RESISTOR NETWORK 1 M U116	1
190642153	RESISTOR NETWORK 15 K U9	1
190642332	RESISTOR NETWORK 3.3 K U6,U79	2
190642473	RESISTOR NETWORK 47 K U117,U118	2

9210 Main Parts List

COMPONENT #	DESCRIPTION REMARKS	QTY
1112		
190832101	RESISTOR NETWORK 100 OHMS U108-U110	3
190842332	RESISTOR NETWORK 3.3 K U71	1
192036102	THERMISTOR 10% 1 K R243	1
200301401	DIODE ARRAY SWITCH DAN401 U101	1
200302401	DIODE ARRAY SWITCH DAP401 U102	1
200331005	IC HEX INVERTER 74HC05 U35	1
200331074	IC D-TYP FLOP 74HCT74 U68,U69,U74	3
200332000	IC 2-INPUT NAND MM74HC00 U25	1
200342138	IC 3-TO-8 LN DEC 74HC138 U66	1
200344131	IC DUAL D M-S FLOP 10H131 U77,U89	2
200373374	IC D-TYP FLOP 74HCT374 U8,U12,U70,U111-U114	7
200442090	IC 650 MHZ PRESCALER 11C90 U119	1
200641259	IC 8-BIT LATCH 74HC259 U78	1
200671373	IC D-TYPE FLOP HCT373 U24,U29,U30,U42	4
205171225	IC 64K NONVOL MEMORY 1225 U53	1
205273256	IC 32K X 8 RAM 62256-10 U22,U40	2
205370001	IC CMOS UV EPROM 27C256 U21 GIVE TO SSD MANUF.	1
205391010	IC 128KX8 EPROM 27C010 U44 (SPARE), U45 GIVE TO SSD MANUF.	1
205752000	IC GAL16V8A-25LP U34 GIVE TO SSD MANUF.	1
205791020	IC GATE ARRAY ACT1020 U27 (PCT303, REV D) TO BE PROGRAMMED BE- FORE INSTALLATION. GIVE TO SSD MANUF.	1
205791020	U28 (PVC302, REV B) TO BE PROGRAMMED BE- FORE INSTALLATION. GIVE TO SSD MANUF.	1
207100301	IC TIMING GENERATOR MTG301 U26,U31,U32,U38,U39 GIVE TO SSD MANUF.	5
207170245	IC 3-STATE BUFFER 74FCT245 U36	1
207244124	IC QUAD TTL-MECL 10H124 U72	1
207244125	IC QUAD MECL-TTL 10H125	1

9210 Main Parts List

COMPONENT #	DESCRIPTION REMARKS	QTY
1112		
	U73	
207257535	IC 14-BIT DAC AD7535 U15,U56-U59	5
207270226	IC QUAD 8-BIT CMOS DAC AD7226 U16	1
207271290	IC 8-CH 12-BIT ADC LTC1290 U103	1
207344164	IC 8-LINE MPLX 10H164 U76,U88	2
207470160	IC BUS TRANSCEIVER 75160B U90	1
207472245	IC BUS TRANSCVR HCT245 U2,U7,U17,U43,U61, U62,U64,U65,U92,U95 U96,U98	12
207490162	IC OCTAL BUS XCVR 75162A U106	1
208011008	IC VOLT COMPARATOR LM311N U120	1
208011011	IC JFET OP AMP TL082CP U13,U18,U19, U48,U51,U86	6
208033001	IC TRANS ARRAY CA3046 U85	1
208110007	IC LO OFFSET OP AMP OP-07 U14,U46,U47,U49,U50, U100,U105	7
208213002	IC VOLT REF +5V REF-02 U104	1
208650689	IC ECL VOLT COMP SPT9689 U87	1
208710694	IC MICRO P SUPRVSR MAX694 U52	1
227168008	IC MICROPROCESSOR 68008 U33	1
227168705	IC MICROPROCESSOR 68705 U3 GIVE TO SSD MANUF.	1
227768901	IC PERIPHERAL 68901 U67	1
227799914	IC GPIB CONTROL TMS9914A U91	1
229020055X	TRANS VOLT SUPPR P6KE6.8 CR27,CR31	2
230110005	DIODE SWITCHING 1N4448 CR16-CR18,CR20,CR21, CR26,CR28-CR30,CR33, CR34	11
235010005	DIODE RECTIFIER 1N4005 CR14	1
253010811	DIODE SCHOTTKY HP2811 CR12,CR13,CR19,CR32, CR35	5
256001071	DIODE LED INFRARED CR1-CR11	11
256500001	DIODE LED RECTANGULAR GRN CR15,CR22-CR25	5
260090711	PHOTO DETECTOR DARLINGTON Q1-Q11	11

9210 Main Parts List

ECO	COMPONENT #	DESCRIPTION REMARKS	QTY
1112			
	270110003	TRANSISTOR NPN PN2222A Q31	1
	270170904X	TRANSISTOR NPN 2N3904 Q15,Q16,Q20,Q22	4
	275110001	TRANSISTOR PNP P2N2907 Q32	1
	275120052	TRANSISTOR PNP BFQ52 Q30	1
	275170906X	TRANSISTOR PNP 2N3906 Q21,Q26-Q29	5
	280120210	TRANSISTOR FET "N" SD210 . Q12	1
	302230101	FILTER CHOKE 1 A 100 UH L1	1
	309040032	CRYSTAL OSCILLATOR 32 MHZ U107	1
	380212181	FOIL COPPER ADHESIVE BACK	0
	400032220	SOCKET IC AUTO INSERTION DIP-20	2
	400042222	SOCKET IC AUTO INSERTION DIP 22	1
	400062228	SOCKET IC AUTO INSERTION DIP 28	2
	400062232	SOCKET IC AUTO INSERTION DIP-32	2
	400062240	SOCKET IC AUTO INSERTION DIP-40	1
	400062248	SOCKET IC AUTO INSERTION DIP-48	1
	400410068	IC SOCKET GRID TYP 68-POS	5
	400419084	IC SOCKET GRID TYPE 84-PIN	2
	402110302	CONN CO-AX PC MTG BNC J1,J2 GIVE TO SSD MANUF.	2
	402610006	CONN CO-AX PC MTG SMB JB4	6
	403950002	POLARIZING KEY	4
	412101112	SWITCH ROT NO STOP 12-POS GIVE TO SSD MANUF.	1
	430530009	RELAY DPDT LATCHING K2	1
	430530010	RELAY SPDT K1	1
	454110002	HDR SOLD TAIL/MALE 2 P7,P8	2
	454110016	HDR SOLD TAIL/MALE 16 P5	1
	454211050	HDR SOLD TAIL/MALE 50 P3 GIVE TO SSD MANUF.	1
	454220020	HDR SOLD TAIL/MALE 20 J5	1
	454221024	HDR SOLD TAIL/MALE 24 P6	1
	454221064	HDR SOLD TAIL/FEM 64 JA,JB	2
	454310060	HDR SOLD TAIL/MALE 60 J13	1
	454311002	HDR SOLD TAIL/MALE 2 J12,J18	2
	454321006	HDR SOLD TAIL/FEM 6 GIVE TO SSD MANUF.	1
	454370002	SHUNT 2 POS	1
	454620050	HDR SOLD TAIL/FEM 50 J3	1

9210 Main Parts List

	COMPONENT #	DESCRIPTION REMARKS	QTY
1112			
	454720060	HDR SOLD TAIL/FEM 60 J4	1
	500110001	TRANSIPAD "SMALL"	2
	510160001	GROUND LUG SPADE TYPE G1-G11,G13,G14 (QTY OF 13 ***	13
	522400606	SPACER ROUND #4 3/16 LONG GIVE TO SSD MANUF.	2
	560256005	SCREW PHILIPS 2-56X5/16	4
	560440008	SCREW PHILIPS 4-40X1/2 GIVE TO SSD MANUF.	2
	560632006	SCREW PHILIPS 6-32X3/8	1
	580256003	NUT ELASTIC STOP HEX 2-56 #####	4
	580440003	NUT ELASTIC STOP HEX 4-40 GIVE TO SSD MANUF.	2
	590551022	WIRE TEFLON 7/30 GRN 22	1
	591552126	WIRE TEF WHT SOLID AWG 26	0
	709210052	BOTTOM PLATE RIGHT SIDE	1
	719210023	PC BD PREASS'Y 9210MAIN	1
	MVL407	MULTI-CH MONO DISC U11	1
	SM270000135	TRANSISTOR NPN BFG135 Q13,Q14	2
	SM275030092	TRANSISTOR PNP BFT92 Q17-Q19,Q23-Q25	6
	SM652101100	RES CHIP (E24) 1% 10 OHMS R9	1
	SM652101102	RES CHIP (E24) 1% 1 K R89	1
	SM652101200	RES CHIP (E24) 1% 20 OHMS R15,R20,R24,R27,R33, R35,R36,R38,R88	9
	SM652101201	RES CHIP (E24) 1% 200 OHMS R85,R86	2
	SM652101241	RES CHIP (E24) 1% 240 OHMS	2
	SM652101300	RES CHIP (E24) 1% 30 OHMS R17,R22	2
	SM653181261	RES THICK FILM 1% 42.2 OHMS	2
	SM661207103	CAP CERA CHIP 20% .01 UF C12,C30,C44,C98,C132 C136,C184,C186	9
	SM661276102	CAP CERA CHIP TESTED .001 UF	2

LECROY 9211/9212/9213/9214
SERVICE MANUAL

General Information

1.0 Introduction

This service manual contains information to maintain the LeCroy 9211/9212/9213/9214 Output Modules. The manual is divided into eight sections as follows:

1. General Information
   Contains the Model 9211/9212/9213/9214 description, specifications, and characteristics.

2. Performance Verification
   Contains the performance tests necessary to verify instrument specifications, including recommended test equipment and test record form.

3. Adjustments / Calibration
   Contains the necessary procedures to adjust the instrument after servicing.

4. Basic Operation / Block Diagrams
   Contains operation descriptions and block diagrams for the instrument.

5. Disassembly
   Contains the disassembly and assembly procedures.

6. Toubleshooting
   Contains troubleshooting flowcharts to assist in the repair of the instrument.

7. Schematics / Reference Drawings
   Contains schematic and component location diagrams.

8. Parts List
   Contains the instuments parts list.

Refer to the LeCroy Model 9210 Operator's Manual for information on operating and programming.

This manual provides replaceable subassembly service information and is not intended to support component level troubleshooting.

1.1 LeCroy 9211
250 MHz, Variable Edge Output Module Specifications

Timing Characteristics:

Maximum Rep Rate: ≥ 50 MHz
Minimum Pulse Width: ≤ 10.0 nsec
Fixed Delay from Trigger Out:
13 nsec ± 4 nsec

Output Characteristics:

Specified with output terminated in 50.00 Ω. (Ratings in { } are when driving an open circuit.)

Output: Normal Polarity
Short Circuit Output Current: ±200 mA
DC Output Source Impedance: 50 ± 2.0 Ω
Output Protection: Protected against application of ≤ ± 40 V

Output Levels:

High Level: -7.98 V to + 8.00 V {-15.96 V to + 16.00 V}
Low Level: -8.00 V to + 7.98 V {-16.00 V to + 15.96 V}

Output Voltage Range: ±8 Volts {±16 Volts}
Max. amplitude of 16 V {32 V}.
Min. amplitude of 20 mV {40 mV}

Resolution: 5 mV {10 mV}

Level Accuracy: ±(1% of programmed value + 1% of Amplitude + 40 mV) into 50.00 Ω
Accuracy with Load Comp: The same accuracy as stated above will be maintained for user supplied load of 47 Ω to 1 MΩ when load compensation feature is enabled.

Pulse Performance:

Variable Transition Times (10% to 90 %):

Leading Edge: ≤ 6.5 nsec to 95 msec
Trailing Edge: ≤ 6.5 nsec to 95 msec

Ranges: 8 ranges of 25:1. Minimum lead to trail dynamic range = 2.5:1 (except for lowest range, see graph below)

Resolution: the greater of 1% or 100 psec

Accuracy: ±(10% of programmed value + 300 psec)

Linearity: ±3% typ. (10-90%) for transition times >100 nsec

Slew Rate mode: Settable down to 0.1 V/msec with 0.1% resolution and ± 10% accuracy (separately settable for leading and trailing edge) Max. rate determined by amplitude setting & transition time limits stated above.

Overshoot and Ringing: the greater of ±8% of amplitude or ± 10 mV

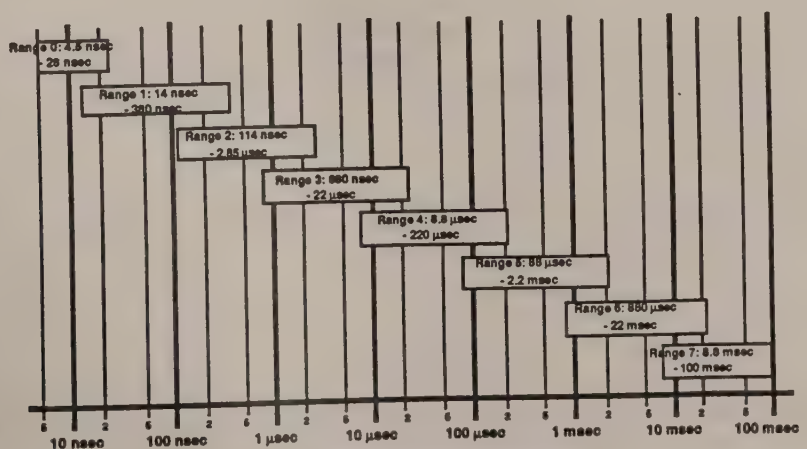
Settling Time: <50 nsec to 2% of amplitude change for amplitudes ≤10 V or to 3% of amplitude change for amplitudes >10 V (at fastest transition times).

Module Controls: *The following controls are located on the front panel of the output module.*

Invert: Inverts normal output pulse levels. Quiescent and active levels exchanged.

Disable: Output circuitry is disconnected via relay.

Display Channel: Instructs mainframe to select and display the settings parameters for this module.



9213 Transition Time Ranges

1.2 LeCroy 9212
300 MHz, 300 ps, Variable Edge Output Module Specifications

Timing Characteristics:

Maximum Rep Rate: ≥ 300 MHz
Minimum Pulse Width: ≤ 1.2 nsec
Maximum Pulse Width:
For Period setting ≤ 8.0 nsec:
Max. Width = Period - 1.4 nsec
For Period setting > 8.0 nsec:
Max. Width = Period - 3.5 nsec
Fixed Delay from Trigger Out:
13 nsec ± 4 nsec

Output Characteristics:

Specified with both outputs terminated in 50.00 Ω. (Ratings in { } are when driving an open circuit.)
Outputs: Normal and Complementary Polarity
Short Circuit Output Current: ±240 mA
DC Output Source Impedance: 50 ± 1.0 Ω
Output Protection: Protected against application of ≤ ± 6 V

Output Levels:

High Level: -4.50V to + 5.00 V {-4.00 V to + 5.00 V}
Low Level: -5.00 V to + 4.50 V {-5.00 V to + 4.00 V}
Output Voltage Range: ±5 Volts {±5 Volts} (Amplitude will double into a high impedance up to the 5 V level limit).
Min. amplitude of 500 mV {1 V}
Max. amplitude of 5 V {10 V}.
Resolution: 5 mV {10 mV}
Level Accuracy:
Normal Output: ±(1% of programmed value + 1% of Amplitude + 40 mV) into 50.00 Ω
Accuracy with Load Comp: The same accuracy as stated above will be maintained for user supplied load of 47 Ω to 1 MΩ when load compensation feature is enabled.
Complementary Output: ±(1% of programmed value + 3% of Amplitude + 40 mV) into 50.00 Ω
Accuracy with Load Comp: ±(3% of programmed value times the ratio of the load on the complemented output to the load on the normal output). Measurements for the load compensating correction factors are made on the normal output.

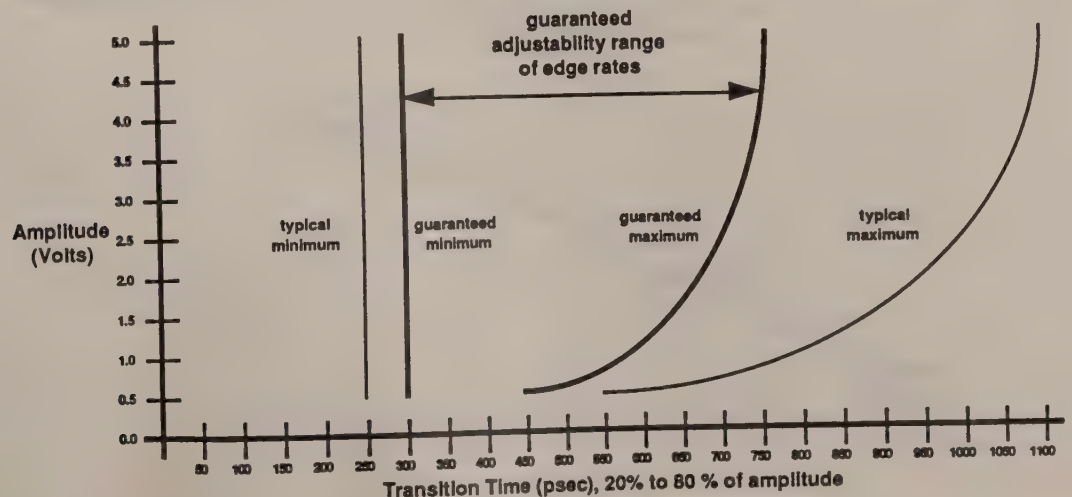
Pulse Performance:

Minimum Transition Time:
≤ 300 psec guaranteed (20% - 80%, @ Lead/Trail programmed for 250 psec)

Maximum Transition Time:

Amplitude	Transition Time @ Lead/Trail set to 1 nsec
0.50 V	≥ 450 psec
0.75 V	≥ 540 psec
1.00 V	≥ 580 psec
2.00 V	≥ 675 psec
3.00 V	≥ 720 psec
4.00 V	≥ 745 psec
5.00 V	≥ 750 psec

Transition Time Accuracy:
±(20% of programmed value + 300 psec) for values less than the maximum)
Transition Time Symmetry:
$|t_{lead}-t_{trail}| < 20\%$ of value ± 300 psec
Transition Time Resolution:
50 psec steps, worst case (at the module output)
Transition Time Repeatability:
± 100 psec (for identical module setup)
Overshoot and Ringing: the greater of ± 8% of amplitude or ± 10 mV
Settling Time: ≤ 10 nsec to 2% of amplitude change at fastest transition time.
Normal to Complemented Output Skew: 100 psec max. at fastest transition time. (25 psec typ.)



1.3 LeCroy 9213
50 MHz, 16 V Amplitude Output Module Specifications

Timing Characteristics:

Maximum Rep Rate: ≥ 250 MHz
Minimum Pulse Width: ≤ 2.0 nsec
Fixed Delay from Trigger Out:
13 nsec ± 4 nsec

Output Characteristics:

Specified with both outputs terminated in 50.00 Ω. (Ratings in { } are when driving an open circuit.)

Outputs: Normal and Complementary Polarity
Short Circuit Output Current: ±260 mA
DC Output Source Impedance: 50 ± 1.0 Ω
Output Protection: Protected against application of ≤ ± 15 V

Output Levels:

High Level: -4.95 V to + 5.00 V {-9.90 V to + 10.00 V}
Low Level: -5.00 V to + 4.95 V {-10.00 V to + 9.90 V}

Output Voltage Range: ±5 Volts {±10 Volts}
Max. amplitude of 5 V {10 V}.
Min. amplitude of 50 mV {100 mV}

Resolution: 5 mV {10 mV}

Level Accuracy:

Normal Output: ±(1% of programmed value + 1% of Amplitude + 40 mV) into 50.00 Ω
Accuracy with Load Comp: The same accuracy as stated above will be maintained for user supplied load of 47 Ω to 1 MΩ when load compensation feature is enabled.

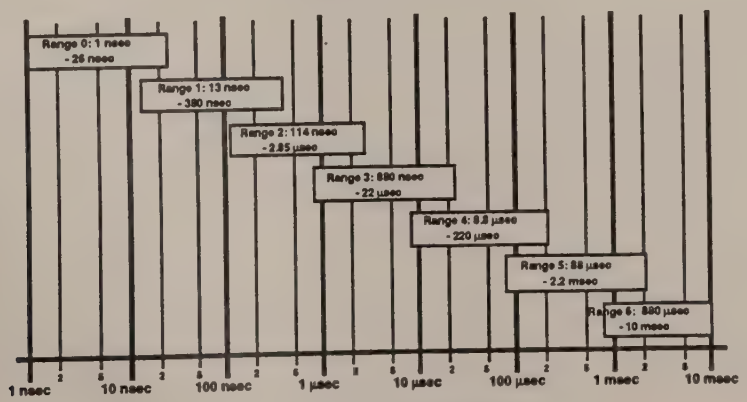
Complementary Output: ±(1% of programmed value + 3% of Amplitude + 40 mV) into 50.00 Ω
Accuracy with Load Comp: ±(3% of programmed value times the ratio of the load on the complemented output to the load on the normal output). Measurements for the load compensating correction factors are made on the normal output.

Pulse Performance:

Variable Transition Times (10% to 90%):
Leading Edge: ≤ 1.2 nsec min (1 nsec typ) to 10 msec
Trailing Edge: ≤ 1.2 nsec min (1 nsec typ) to 10 msec
Ranges: 7 ranges of 25:1. Minimum lead to trail dynamic range = 2.5:1, except 2:1 at first range break (see graph below)
Resolution: the greater of 1% or 100 psec
Accuracy: ±(10% of programmed value + 300 psec)
Linearity: ±3% typ. (10-90%) for transition times > 50 nsec
Slew Rate mode: Settable down to 0.1 V/msec with 0.1% resolution and ± 10% accuracy (separately settable for leading and trailing edge) Max. rate determined by amplitude setting & transition time limits stated above.
Overshoot and Ringing: the greater of ± 8% of amplitude or ±10 mV
Settling Time: ≤ 10 ns to 2% of amplitude change at fastest transition times
Normal to Complementary Output Skew: 200 psec max at fastest transition times. (50 psec typ)

Module Controls: *The following controls are located on the front panel of the output module.*

Invert: Inverts normal output pulse levels. Quiescent and active levels exchanged.
Disable: Output circuitry is disconnected via relay.
Display Channel: Instructs mainframe to select and display the settings parameters for this module.



9211 Transition Time Ranges

LECROY 9211/9212/9213/9214 OUTPUT MODULE
Performance Verification Procedure

2.0 Introduction

This procedure can be used to verify the main operating specifications of the LeCroy 9211, 9212 9213, or 9214 pulse generator output modules. It is useful as a calibration verification procedure as well as an incoming inspection checkout.

Equipment Required

Description	Performance Requirements	Recommended Models
Time interval counter (TIC)	300 MHz frequency A to B, Period, width, rise, fall interval accuracy <2.5ns	**Stanford Research Systems 620** HP 5335A HP 5334B A digital oscilloscope with adequate accuracy may be used.
Digital Multimeter	4 1/2 digit	**HP 3478A**
Sampling Scope	5 GHz bandwidth	**TEK 7603 with 7T11/7S11 & S-2** HP 54120 series TEK 11800 series
LeCroy 9210 Pulse Generator Mainframe		**LeCroy 9210**

Preliminary setup

1. Install module in Channel A slot of 9210.
2. Power up 9210 and allow at least 15 minute warmup period.
3. Retrieve default setup in the pulse generator. Do this on the pulse generator by recalling the standard settings. The following default settings will be applied:

setting	value	change	setting	value	change
CHANNEL:			**TRIGGER:**		
Amplitude	500 mV		Mode	Normal	
Median	0		Burst count	3	
Duty cycle	20%		Level	.1V	
Delay	0		Slope	+	
Lead	1 ns				
Trail	1 ns		**MODULE:**		
Period	100 ns		Invert	off	
			Disable	on	

2.1 Self Test

1. Bring up the "MORE" menu on 9210 and press "CAL" to intiate self-calibration.
2. Check that unit passed self calibration. Enter result on Test Report.
3. Bring up the "MORE" menu on 9210 and press "SELF TEST" to initiate self test.
4. Check that unit passed self test. Enter result on Test Report.

2.2 Output Level DC Accuracy

Specification:

Summary:

The pulse generator output level DC accuracy is checked with a DMM. The upper or lower level is held by placing the pulse generator in external width mode with no trigger input. The upper and lower levels are selected by setting the trigger slope to negative and positive values respectively.

Equipment:

1. DMM

Setup:

1. Press "RECALL SETUP" on front panel. Select "STANDARD". Enable Module outputs.
2. Adjust settings of pulse generator as shown in table below. Note that only settings with an x in the change column need to be change if you are following the order of the procedure.

setting	value	change	setting	value	change
CHANNEL:			TRIGGER:		
Vhigh	5.0	x	Mode	E. Wid	x
Vlow	0	x	Burst count	3	
Duty cycle	20%		Level	1V	
Delay	0		Slope	-	
Lead	1 ns				
Trail	1 ns		MODULE:		
Period	100 ns		Invert	off	
			Disable	off	x

3. Cable output of 9211/12/13/9214 to voltage measuring input of DMM.The input termination of the DMM must be 50 Ω ± .1%. If a .1% termination is unavailable, the following formula can be used to compensate the termination.

$$\frac{0.5}{[\text{termination}/(\text{termination} + 50.00)]} = \text{Compensation Factor}$$

Multiply the DMM readings by the compensation factor to obtain the true voltage reading.

4. On modules with two outputs, the OUT must be terminated into 50Ω.

Procedure:

1. Make sure pulse generator trigger mode is set to ext width and slope is negative to force high level output.
2. Set Vlow to 0.0 V .
3. Set Vhigh to voltage in next test step shown in test record.
4. Record measurement on DMM in test record and check limits.
5. Repeat steps 3 and 4 above for lines 2.2 to 2.6 of the test record (9211).

   lines 2.2 to 2.4 of the test record (9212 and 9214).
   lines 2.2 to 2.7 of the test record (9213).
6. Set trigger slope positive to force low level output.
7. Set Vhigh to 0.0 V.
8. Set Vlow to voltage in next test step shown in test record.
9. Record DMM measurement in test record and check limits.
10. Repeat steps 8 and 9 above for lines 2.8 to 2.12 of the test record (9211).

    lines 2.6 to 2.8 of the test record (9212 and 9214).

    lines 2.8 to 2.14 of the test record (9213).

2.3 Long Transition Time and Accuracy Test (10% - 90%) (only for 9211 and 9213, not for 9212 or 9214)

Specification:

Accuracy of 10%-90% transition time: ± 10% of setting

Summary:

Transition times in the range of 100 nsec to 10 msec are measured using the time interval counter.

Equipment:

1. Time interval counter

Setup:

1. Set pulse generator settings as shown in table below.

setting	value	change	setting	value	change
CHANNEL:			TRIGGER:		
Amplitude	5.0		Mode	Normal	x
Median	0		Burst count	3	
Duty cycle	50%	x	Level	0.1V	
Delay	0		Slope	+	
Lead	100 ns	x			
Trail	100 ns	x	MODULE:		
Period	100 ms	x	Invert	off	
			Disable	off	

2. Set time interval counter as indicated below:

Setting	Value
Mode	rise
A Trigger level	-2.0V
A Trigger slope	+
A coupling	DC, 50 ohm term
B Trigger level	+2.0V
B Trigger slope	+
B Coupling	DC, 50 ohm term

Procedure:

1. Set pulse generator to the leading edge transition time shown in next step of the Test Record.
2. Record measurement from time interval counter in Test Record and check limits.
3. Repeat steps 1 and 2 for lines 3.2 to 3.8 of the Test Record
4. Set leading edge transition time to 100 nsec.
5. Set trailing edge transition time to time shown in next step of test record.
6. Record measurement from time interval counter in test record and check limits.
7. Repeat steps 5 and 6 for lines 3.2 to 3.8 of the test record.

2.4 Short Transition Time Accuracy Test (only 9211 and 9213, not for 9212 or 9214)

Specification:

Accuracy of 10%-90% transition time: ± 10% of setting

Summary:

Transition times in the range of 1 nsec to 20 nsec are measured using the sampling oscilloscope. The measurements may be done manually or automatically depending on what type of sampling scope is available.

Equipment:

1. Sampling oscilloscope

Setup:

1. Set pulse generator settings as shown in table below.

setting	value	change	setting	value	change
CHANNEL:			TRIGGER:		
Amplitude	5.0		Mode	Normal	
Median	0		Burst count	3	
Duty cycle	50%	x	Level	0.1V	
Delay	0		Slope	+	
Lead	20 ns	x			
Trail	20 ns	x	MODULE:		
Period	100 ns	x	Invert	off	
			Disable	off	

2. Cable 9211 output to sampling scope.

Procedure:

1. Set pulse generator to the leading and trailing edge transition times shown in next step of the Test Record.
2. Measure the 10%-90% leading edge transition time. Final measurement should be within 1 minor division with scope time/division set to value in test record (t/div).
3. Center trailing edge transition on scope screen and measure the 10%-90% trailing edge transition time.
4. Repeat steps 1 to 3 for lines 4.3 to 4.6 of the Test Record

2.5 9212 and 9214 Transition Time Range Test (20% - 80%)

Specification:

Summary:

Check that transition time range is achievable at 2 amplitude values. Transition times in the range of 0.3 nsec to 1 nsec are measured using the sampling oscilloscope. The measurements may be done manually or automatically depending on what type of sampling scope is available.

Equipment:

1. Sampling oscilloscope

Setup:

1. Set pulse generator settings as shown in table below.

setting	value	change	setting	value	change
CHANNEL:			TRIGGER:		
Amplitude	5.0		Mode	Normal	
Median	0		Burst count	3	
Duty cycle	50%		Level	0.1V	
Delay	0		Slope	+	
Lead	0.3 ns	x			
Trail	0.3 ns	x	MODULE:		
Period	100 ns		Invert	off	
			Disable	off	

2. Cable 9212 output to sampling scope.

Procedure:

1. Set pulse generator to the edge transition time shown in next step of the Test Record.
2. Measure the 20%-80% leading edge transition time. Final measurement should be within 1 minor division with scope time/division set to value in test record (t/div).
3. Center trailing edge transition on scope screen and measure the 20-80 trailing edge transition time.
3. Repeat steps 1 to 3 for lines 5.2 to 5.8 of the Test Record

2.6 Overshoot

Specification:

Overshoot and ringing less than 8% of amplitude.

Summary:

Overshoot and ringing at minimum transition time are measured for both the leading and trailing edge transitions at two amplitudes using the sampling oscilloscope . The measurements may be done manually or automatically depending on what type of sampling scope is available.

Equipment:

1. Sampling oscilloscope

Setup:

1. Set pulse generator settings as shown in table below.

setting	value	change	setting	value	change
CHANNEL:			TRIGGER:		
Amplitude	5.0		Mode	Normal	
Median	0		Burst count	3	
Duty cycle	50%		Level	0.1V	
Delay	0		Slope	+	
Lead	1 ns	x			
Trail	1 ns	x	MODULE:		
Period	100 ns	x	Invert	off	
			Disable	off	

2. Cable output module to sampling scope.

Procedure:

1. Set the amplitude for the next test step according to the test record and find edge.
2. Center the edge to be measured on the scope screen and adjust the time/division so that the after transition settling region is maximally visible.
3. The measured overshoot for this test is the maximum excursion away from the final settled value after the initial transition passes through the 92% point. Note that by this definition it can be negative (ring back). Measure the maximum deviation from the final settled value and enter that voltage difference in the test record.
4. Repeat steps 1 to 3 for lines 6.2 to 6.4 of the test record.

2.7 9211 PERFORMANCE VERIFICATION TEST RECORD

TESTED BY: _____ PASSED:____ FAILED:____

SERIAL NUMBER: _____ DATE: _____

COMMENTS:

_____

_____

_____

_____

2.7.1 Self Test

1.1 Self Calibration Pass____ Fail____

1.2 Self Test Pass____ Fail____

_____

2.7.2 Output Level DC Accuracy

Step	Set Vlow	Set Vhigh	Lower Limit	Measured Level	Upper Limit	Pass	Fail
2.1	0.0	5.0	4.86 V	_____	5.14 V	____	____
2.2	0.0	3.0	2.9 V	_____	3.1 V	____	____
2.3	0.0	1.0	0.94 V	_____	1.06 V	____	____
2.4	0.0	0.5	0.45 V	_____	0.55 V	____	____
2.5	0.0	0.3	254 mV	_____	346 mV	____	____
2.6	0.0	0.1	58 mV	_____	142 mV	____	____
2.7	-5.0	0.0	-5.8 V	_____	-4.86 V	____	____
2.8	-3.0	0.0	-3.1 V	_____	-2.9 V	____	____
2.9	-1.0	0.0	-1.06 V	_____	-0.94 V	____	____
2.10	-0.5	0.0	-0.55 V	_____	-0.45 V	____	____
2.11	-0.3	0.0	-346mV	_____	-254 mV	____	____
2.12	-0.1	0.0	-142mV	_____	-58mV	____	____

2.7.3 Long Transition Time Range Test (10% - 90%)

Step	Set Transition	Lower Limit	Measured Trans. time (10-90)	Upper Limit	Pass	Fail
Leading Edge						
3.1a	100ns	90 ns	_____	110 ns	____	____
3.2a	1 us	0.9 us	_____	1.1 us	____	____
3.3a	10 us	9 us	_____	11 us	____	____
3.4a	100 us	90 us	_____	110 us	____	____
3.5a	1 ms	900 us	_____	1.1 ms	____	____
3.6a	10 ms	9 ms	_____	11 ms	____	____
Trailing Edge						
3.1b	100ns	90 ns	_____	110 ns	____	____
3.2b	1 us	0.9 us	_____	1.1 us	____	____
3.3b	10 us	9 us	_____	11 us	____	____
3.4b	100 us	90 us	_____	110 us	____	____
3.5b	1 ms	900 us	_____	1.1 ms	____	____
3.6b	10 ms	9 ms	_____	11 ms	____	____

2.7.4 Short Transition Time Accuracy Test (10%-90%)

Step	Set Trans	Edge	Scope Time/Div	Lower Limit	Measured Trans. time (10-90)	Upper Limit	Pass	Fail
4.1	1 ns	Lead	500 psec/div	0.6 ns	_____	1.4 ns	____	____
4.2	1 ns	Trail	500 psec/div	0.6 ns	_____	1.4 ns	____	____
4.3	10 ns	Lead	1 nsec/div	8.7 ns	_____	11.3 ns	____	____
4.4	10 ns	Trail	1 nsec/div	8.7 ns	_____	11.3 ns	____	____
4.5	20 ns	Lead	2 nsec/div	17.7 ns	_____	22.3 ns	____	____
4.6	20 ns	Trail	2 nsec/div	17.7 ns	_____	22.3 ns	____	____

Test 2.7.5 is not performed for the 9211

2.7.6 OVERSHOOT

Step	Set Ampl	Meas Edge	Lower Limit	Measured Overshoot (V)	Upper Limit	Pass	Fail
6.1	5 V	Lead	-0.4 V	_____	0.4 V	____	____
6.2	5 V	Trail	-0.4 V	_____	0.4 V	____	____
6.3	1 V	Lead	-80 mV	_____	80 mV	____	____
6.4	1 V	Trail	-80 mV	_____	80 mV	____	____

2.8 9212 PERFORMANCE VERIFICATION TEST RECORD

TESTED BY: _____ PASSED:____ FAILED:____

SERIAL NUMBER: _____ DATE: _____

COMMENTS:

_____

_____

_____

_____

2.8.1 Self Test

1.1 Self Calibration Pass____ Fail____

1.2 Self Test Pass____ Fail____

_____

2.8.2 Output Level DC Accuracy

Step	Set Vlow	Set Vhigh	Lower Limit	Measured Period	Upper Limit	Pass	Fail
2.1	0.0	5.0	4.86 V	_____	5.14 V	____	____
2.2	0.0	3.0	2.9 V	_____	3.1 V	____	____
2.3	0.0	1.0	0.94 V	_____	1.06 V	____	____
2.4	0.0	0.5	0.45 V	_____	0.55 V	____	____
2.5	-5.0	0.0	-5.14 V	_____	-4.86 V	____	____
2.6	-3.0	0.0	-3.1 V	_____	-2.9 V	____	____
2.7	-1.0	0.0	-1.06 V	_____	-0.94 V	____	____
2.8	-0.5	0.0	-0.55 V	_____	-0.45 V	____	____

_____

Tests 2.8.3 through 2.8.4 are not performed on 9212.

_____

2.8.5 9212 Transition Time Range Test (20% - 80%)

Step	Set Ampl	Meas Edge	Set Lead	Scope Time/Div	Lower Limit	Measured Trans. time	Upper Limit	Pass	Fail
5.1	5 V	Lead	250 ps	50 ps	------	_____	300 ps	____	____
5.2	5 V	Lead	1 ns	200 ps	750 ps	_____	-------	____	____
5.3	5 V	Trail	250 ps	50 ps	------	_____	300 ps	____	____
5.4	5 V	Trail	1 ns	200 ps	750 ps	_____	-------	____	____
5.5	1 V	Lead	250 ps	50 ps	------	_____	300 ps	____	____
5.6	1 V	Lead	1 ns	200 ps	580 ps	_____	-------	____	____
5.7	1 V	Trail	250 ps	50 ps	------	_____	300 ps	____	____
5.8	1 V	Trail	1 ns	200 ps	580 ps	_____	-------	____	____

2.8.6 Overshoot

Step	Set Ampl	Meas Edge	Lower Limit	Measured Overshoot (V)	Upper Limit	Pass	Fail
6.1	5 V	Lead	-0.4 V	_____	0.4 V	____	____
6.2	5 V	Trail	-0.4 V	_____	0.4 V	____	____
6.3	1 V	Lead	-80 mV	_____	80 mV	____	____
6.4	1 V	Trail	-80 mV	_____	80 mV	____	____

2.9 9213 PERFORMANCE VERIFICATION TEST RECORD

TESTED BY: _____ PASSED:____ FAILED:____

SERIAL NUMBER: _____ DATE: _____

COMMENTS:

_____

_____

_____

_____

2.9.1 Self Test

1.1 Self Calibration Pass____ Fail____

1.2 Self Test Pass____ Fail____

_____

2.9.2 Output Level DC Accuracy

Step	Set Vlow	Set Vhigh	Lower Limit	Measured Level	Upper Limit	Pass	Fail
2.1	0.0	8.0	7.8 V	_____	8.2 V	____	____
2.2	0.0	5.0	4.86 V	_____	5.14 V	____	____
2.3	0.0	3.0	2.9 V	_____	3.1 V	____	____
2.4	0.0	1.0	0.94 V	_____	1.06 V	____	____
2.5	0.0	0.5	0.45 V	_____	0.55 V	____	____
2.6	0.0	0.3	254 mV	_____	346 mV	____	____
2.7	0.0	0.1	58 mV	_____	142 mV	____	____
2.8	-8.0	0.0	-8.2 V	_____	-7.8 V	____	____
2.9	-5.0	0.0	-5.14 V	_____	-4.86 V	____	____
2.10	-3.0	0.0	-3.1 V	_____	-2.9 V	____	____
2.11	-1.0	0.0	-1.06 V	_____	-0.94 V	____	____
2.12	-0.5	0.0	-0.55 V	_____	-0.45 V	____	____
2.13	-0.3	0.0	-346 mV	_____	-254 mV	____	____
2.14	-0.1	0.0	-142 mV	_____	-58 mV	____	____

2.9.3 Long Transition Time Accuracy Test (10% - 90%)

Step	Set Transition	Lower Limit	Measured Trans. time (10%-90%)	Upper Limit	Pass	Fail
Leading Edge						
3.1a	100 ns	90 ns	_____	110 ns	____	____
3.2a	1 us	0.9 us	_____	1.1 us	____	____
3.3a	10 us	9 us	_____	11 us	____	____
3.4a	100 us	90 us	_____	110 us	____	____
3.5a	1 ms	900 us	_____	1.1 ms	____	____
3.6a	10 ms	9 ms	_____	11 ms	____	____
3.7a	95 ms	85.5 ms	_____	104.5 ms	____	____
Trailing Edge						
3.1b	10 ns	90 ns	_____	110 ns	____	____
3.2b	1 us	0.9 us	_____	1.1 us	____	____
3.3b	10 us	9 us	_____	11 us	____	____
3.4b	100 us	90 us	_____	110 us	____	____
3.5b	1 ms	900 us	_____	1.1 ms	____	____
3.6b	10 ms	9 ms	_____	11 ms	____	____
3.7b	95 ms	85.5 ms	_____	104.5 ms	____	____

2.9.4 Short Transition Time Accuracy Test (10%-90%)

Step	Set Trans	Edge	Scope Time/Div	Lower Limit	Measured Trans. time (10-90)	Upper Limit	Pass	Fail
4.1	6.5 ns	Lead	500 psec/div	5.55 ns	_____	7.45 ns	____	____
4.2	6.5 ns	Trail	500 psec/div	5.55 ns	_____	7.45 ns	____	____
4.3	10 ns	Lead	1 nsec/div	8.7 ns	_____	11.3 ns	____	____
4.4	10 ns	Trail	1 nsec/div	8.7 ns	_____	11.3 ns	____	____
4.5	20 ns	Lead	2 nsec/div	17.7 ns	_____	22.3 ns	____	____
4.6	20 ns	Trail	2 nsec/div	17.7 ns	_____	22.3 ns	____	____

Test 2.9.5 is not performed for the 9213

2.9.6 OVERSHOOT

Step	Set Ampl	Meas Edge	Lower Limit	Measured Overshoot (V)	Upper Limit	Pass	Fail
6.1	5V	Lead	-0.4 V	_____	0.4 V	____	____
6.2	5V	Trail	-0.4 V	_____	0.4 V	____	____
6.3	1V	Lead	-80 mV	_____	80 mV	____	____
6.4	1V	Trail	-80 mV	_____	80 mV	____	____

2.10 9214 PERFORMANCE VERIFICATION TEST RECORD

TESTED BY: _____ PASSED:____ FAILED:____

SERIAL NUMBER: _____ DATE: _____

COMMENTS:

_____

_____

_____

_____

2.10.1 Self Test

1.1 Self Calibration Pass____ Fail____

1.2 Self Test Pass____ Fail____

_____

2.10.2 Output Level DC Accuracy

Step	Set Vlow	Set Vhigh	Lower Limit	Measured Period	Upper Limit	Pass	Fail
2.1	0.0	5.0	4.86 V	_____	5.14 V	____	____
2.2	0.0	3.0	2.9 V	_____	3.1 V	____	____
2.3	0.0	1.0	0.94 V	_____	1.06 V	____	____
2.4	0.0	0.5	0.45 V	_____	0.55 V	____	____
2.5	-5.0	0.0	-5.14 V	_____	-4.86 V	____	____
2.6	-3.0	0.0	-3.1 V	_____	-2.9 V	____	____
2.7	-1.0	0.0	-1.06 V	_____	-0.94 V	____	____
2.8	-0.5	0.0	-0.55 V	_____	-0.45 V	____	____

_____

Tests 2.10.3 through 2.10.4 are not performed on 9214.

_____

2.10.5 9214 Transition Time Range Test (20% - 80%)

Step	Set Ampl	Meas Edge	Set Lead	Scope Time/Div	Lower Limit	Measured Trans. time	Upper Limit	Pass	Fail
5.1	5 V	Lead	250 ps	50 ps	------	_____	300 ps	____	____
5.2	5 V	Trail	250 ps	50 ps	------	_____	300 ps	____	____
5.3	1 V	Lead	250 ps	50 ps	------	_____	300 ps	____	____
5.4	1 V	Trail	250 ps	50 ps	------	_____	300 ps	____	____

2.10.6 Overshoot

Step	Set Ampl	Meas Edge	Lower Limit	Measured Overshoot (V)	Upper Limit	Pass	Fail
6.1	5 V	Lead	-0.4 V	_____	0.4 V	____	____
6.2	5 V	Trail	-0.4 V	_____	0.4 V	____	____
6.3	1 V	Lead	-80 mV	_____	80 mV	____	____
6.4	1 V	Trail	-80 mV	_____	80 mV	____	____

ADJUSTMENTS / CALIBRATION

3.0 Introduction

This section includes the adjustments required for the instrument. It is recommended that they be verified at one year intervals.

NOTE ***If it is not possible to make any of the following adjustments, refer to the troubleshooting section of this manual.***

3.1 Equipment Requirements

Instrument	Specification
DVM	4.5 digits
Oscilloscope	300 Mhz bandwidth

3.2 LeCroy 9211 Adjustments

1. No service adjustments.

3.3 LeCroy 9212 Adjustments

1. No service adjustments

3.5 LeCroy 9213 Adjustments

Setup

1. Remove the PC Board (9213PCB) from the 9213 Output Module (see Sect. 5.1 Disassembly).

2. Remove the Top Cover of the LeCroy 9210 Mainframe (see Sect. 5 Disassembly).

Setup (Continued)

3. Insert the 9213 Output Module into the LeCroy 9210 Mainframe and power on the unit. Allow a 15 minute warm up period. Set the 9210 as follows:

Channel A or B		Trigger	
Amplitude	10V	Mode	Normal
Median	0mV	Burst	3
Duty Cycle	50%	Level	-0.50V
Lead	4.50ns	Slope	Positive
Trail	4.50ns		
Period	20ms		
Vmax	500mV		
Vmin	-500mV		

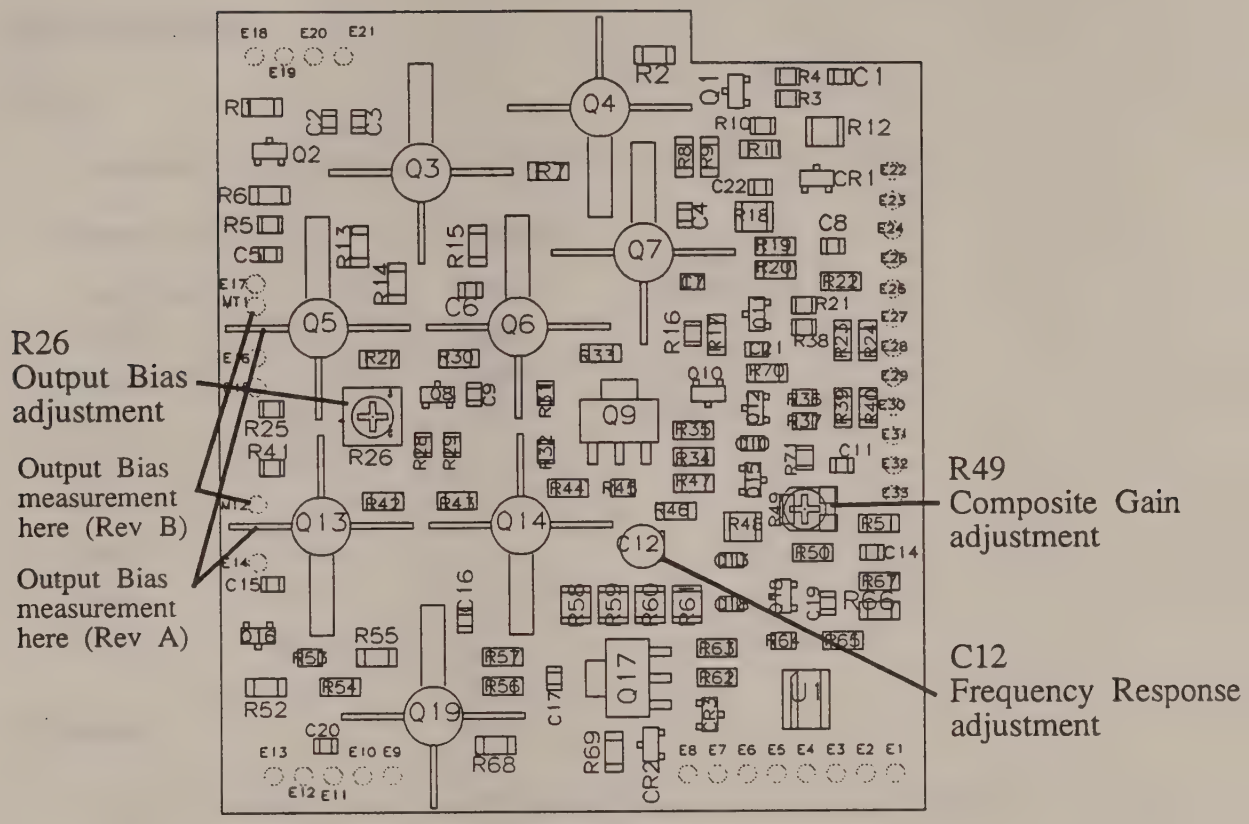
2. Connect the Output Module to the Oscilloscope. Set the Oscilloscope as follows: 5 ms per div., 5 V per div., 50 Ω input termination.

Output Bias Adjustment

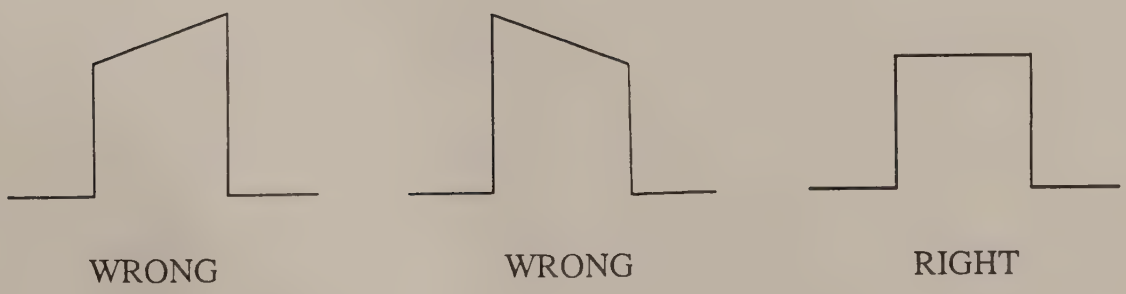
1. Using a DVM, Adjust R26 on the 9213AMP PC Board (see fF3.5.1) for 2.0v ± 20 mV. Measurement is taken between the bases of Q5(+) and Q13(-) as shown in F3.5.1.

Composite Gain Adjust

1. Adjust R49 (see F3.5.1) on the 9213AMP PC Board for flattest response as shown in F3.5.2.



F3.5.1 9213 AMP PC Board Adjustments



F3.5.2 Composite Gain Adjustment

Frequency Response

Setup

1. Re-calibrate the instrument and set the LeCroy 9210 Mainframe as follows:

Channel A or B		Trigger	
Amplitude	5 V	Mode	Normal
Median	0 mV	Burst	3
Duty Cycle	50%	Level	-0.50 V
Delay	0 ns	Slope	Positive
Lead	4.50 ns		
Trail	4.50 ns		
Period	100 ns		
Vmax	500 mV		
Vmin	-500 mV		

Adjustment

1. Adjust C12 (see F3.5.1.) on the 9213 AMP PC Board for approx 2% overshoot.

3.6 LeCroy 9214 Adjustments

1. No service adjustments

MODULES BASIC OPERATION

4.0 General Description

There are certain characteristics that are common to all modules. These will be outlined here. The timing input is a differential ECL source terminated 50 Ω transmission line. On each module this signal is also terminated with 50 Ω in order to minimize possible errors due to transmission line effects. Therefore at the termination resistor the signal level is ≈400 mV p-p.

The digital interface is also very similar on each module. Module decoding and DTACK generation (see 9210 section 4, Basic Operation) is provided by the PCT303 FPGA on the main board. The timing to the modules is purposely made long (≈1 uS) in order to accomodate whatever may be in the modules since the DTACK signal is not generated on the module. Each module contains various registers, DACs and other miscellaneous hardware to which data is written. Modules also contain an EPROM that has the code required to control the module's functions. The hardware and EPROM occupy the same address space with all microprocessor READs being EPROM accesses and all WRITEs being hardware accesses.

A module is detected as being in place by the keypad scan. Once the module is detected as being in place, the microprocessor attempts to read the module's EPROM. If the EPROM contains data of the correct format, the microprocessor "knows" that the EPROM contains the code to control the module and it begins executing the setup and calibration code. If the module is in place on system power up, the mainframe is calibrated first and then each module in turn (A then B) .

Another common signal is the timing readback. It is used primarily for calibration of transition times of the module. The analog readback is an analog voltage that is used by the calibration system to measure various voltages on the module.

The base address for each module is determined by the POD_SEL* signal from the mainframe. Module A's base address is 80000 hex and module B's base address is 88000 hex.

A note of caution; since the system is auto calibrated it can be looked at as a closed loop system only during its calibration cycle. If there are any faults in the calibration feedback loops, strange behavior may result. As a result, care should be taken to verify all settings when troubleshooting. See section 6, TROUBLESHOOTING for more detailed information.

9211 BASIC OPERATION

4.1 General Description (Block Diagram Figure 4.1)

On the 9211, most of the signal path and signal fidelity determining functions are contained in the two hybrids, HSC309 and HVV304. The HSC309 is responsible for receiving the input timing signal, adjusting the transition time, fine amplitude control, signal inversion, a 10 db attenuator, and level shifting the signal to be compatible with the HVV304 input. The HVV304 is a power amplifier with approximately 400 MHz of bandwidth capable of driving 5 Vp-p into 50 ohms. Its single ended voltage gain is fixed at about 5.4.

In general the signal is adjustable, via a DAC under microprocessor control, over a 5 db range (1.778:1). Therefore at 5 db increments throughout the range of amplitude operation an attenuator is switched into the signal path. This means there are 5 db, 10 db and 20 db attenuators for a maximum attenuation of 35 db. The 5 db attenuator is comprised of surface mount components on the solder side of the PCB between the HSC309 and HVV304 hybrids. The 10 db attenuator is inside the HSC309 and the 20 db attenuator is a network at the output of the HVV304. In order to maintain the full range of offset with the 20 db attenuator in place a separate offset voltage, Voffset 2, is generated and applied to the 20 db attenuator network when it is switched in (≤505 mV requested output amplitude).

The remainder of the circuitry on the 9211 is output overvoltage protection and support circuitry (DACs and measurement circuitry) to provide control to the hybrids.

A note of caution; since the system is auto calibrated it can be looked at as a closed loop system only during its calibration cycle. If there are any faults in the calibration feedback loops, strange behavior may result. As a result, care should be taken to verify all settings when troubleshooting. See section 6, TROUBLESHOOTING for more detailed information.

4.1.1 HSC309 (Block Diagram Figure 4.1.1)

The HSC309 is comprised of the MSG305 (a custom designed IC), various capacitors and switches for different ranges of transition time programming, a complement switch and a 10 db attenuator. The entire signal path is differential.

A great deal of the functionality of the HSC309 is contained in the MSG305 as described below. The remainder of the HSC309 is comprised of emitter followers to buffer the MSG305 output and drive a PNP differential pair. The complement switch is implemented by either steering the output current from the differential pair straight through (normal) or cross-coupling the output current (inverted). The 10 db attenuator is a 50 ohm PI atttenuator network.

This "stack" of PNP stages also has the effect of shifting the DC level to ≈13 Volts. This is the level required to drive the HVV304.

4.1.2 MSG305 (Block Diagram Figure 4.1.2)

The purpose of the MSG305 is to accept the timing input and generate a signal with the requested rise and fall times. Additionally, the MSG305 is used to adjust the signal amplitude in small steps (<5 mV at the output) over a 5 db range. The MSG305 is capable of generating output rise and fall times as fast as 650 ps.

The operation of the MSG305 is reasonably straightforward. Timing inputs are accepted and conditioned to drive current switches. The currents that are switched are mirrored from input currents. These are the IRIN (I Rise IN) and IFIN (I Fall IN) inputs. The signal swings from VBOT to VTOP (which are nominally set at ± 538 mV) at a rate equal to the current divided by the equivalent capacitance. Since the current is variable over a large range (40 ua to 4 ma at the ICs internal node), the limiter employs a compensation scheme to cancel any variation in the limiting voltage as the current changes. There is a residual effect of about 10 - 20 mV that is measured and compensated for in firmware. The signal is buffered by a switchable input buffer whose input is a PNP emitter follower and applied to the output variable gain stage. A bias cancellation current (IINTZ) is input to cancel the PNP base current. This can vary from ≈20 uA to ≈120 uA from chip to chip. The output of the buffer is isolated by a large (4 kohm) resistor and sent off the chip as TSOUT. This signal is used as the comparison signal in the thermal tail compensation circuit as well as being used during calibration to eliminate chip to chip variations in offsets.

The MSG305 output stage is a current multiplying gain stage capable of gain variation over ≈2:1 range. It is a differential stage with the other input being AIN*. This input is used as the thermal compensation input. After a transition, the thermal effect is to cause the signal to increase in amplitude, usually with a long time constant. By applying a signal to AIN* and hence decreasing the input signal, the output signal amplitude is decreased.

Finally, a diode bridge switch is used to isolate the very high speed internal signal path from the external capacitors. This is so that the stray capacitance associated with the hybrid and additional capacitors does not slow down the very high speed edges. When the bridge is ON, the capacitors that exist in the HSC309 can be switched in to allow longer transition times to be programmed.

4.1.3 HVV304 (Block Diagram Figure 4.1.3)

The HVV304 is the output amplifier/driver circuit. Its gain is approximately 5.4. It is comprised of emitter followers to drive a differential pair whose current is driven into a common base stage. The common base stage is used to isolate the collectors of the wideband differential pair from the output. Also, the transistors used in the common base stage have a higher collector to base breakdown voltage than the differential pair transistors. In order to maintain sufficient operating headroom on the transistors, the input is required to be at approximately -13 volts. (Recall that the output is capable of swinging to -10 volts into an open circuit.)

The HVV304 also exhibits a thermal settling tail. Since the effect of the thermal response is to cause the output signal to get larger, a signal is summed into the thermal compensation circuit the causes the output signal to reduce, thereby compensating for the thermal tail.

Finally, the 50Ω back termination resistors for OUTPUT and OUTPUT* are on the HVV304 substrate.

4.2 General Description (Block Diagram Figure 4.2)

Most of the 9212 functionality is implemented in the HLV308 hybrid. The HLV308 is responsible for adjusting the transition time, output amplitude and output offset. The Pulse Shrink circuit is responsible for decreasing ("shrinking") the minimum pulse width to under 1.2 ns. The rest of the 9212 is support circuitry for the HLV308.

A note of caution; since the system is auto calibrated it can be looked at as a closed loop system only during its calibration cycle. If there are any faults in the calibration feedback loops, strange behavior may result. As a result, care should be taken to verify all settings when troubleshooting. See section 6, TROUBLESHOOTING for more detailed information.

4.2.1 HLV308 (Block Diagram Figure 4.2.1)

The HLV308 is comprised of an input differential pair, a level-shifting and reversing switch stage, the Pin Driver IC and the output amplifier. The entire signal path is differential. The input differential pair together with the level-shifting/reversing switch stage generates the input signal to the Pin Driver. The COMPLEMENT* control (TTL-level) is implemented by the reversing switch, and causes to be active either the Pin Driver normal input (COMPLEMENT* = Logic 1), or the Pin Driver complement input (COMPLEMENT* = Logic 0).

The Pin Driver is actually two separate devices on the same die. Each device has a differential input, edge rate control and single-ended output. In order to achieve a differential signal out of the Pin Driver, the two devices are used in a complementary fashion (ie. the "+" input of the "A" device is tied to the "-" input of the "B" device and vice versa). The Pin Driver is responsible for adjusting the transition time and the amplitude of the drive signal to the HLV308 output amplifier. The transition time is adjusted by varying the voltages on the ERCA ("A" Pin Driver Edge Rate Control) and ERCB ("B" Pin Driver Edge Rate Control) pins. These voltages are variable between two of the Pin Driver supply voltages, VSS and VEE. The minimum transition time (maximum edge rate) is achieved when the voltages on ERCA and ERCB are equal to VSS. The maximum transition time

(minimum edge rate) is achieved when the voltages on ERCA and ERCB are equal to VEE. The amplitude of the signal out of the Pin Driver is adjusted by varying the VHI and VLO supplies. Each of the two Pin Driver devices has its own set of VHI and VLO supplies (VHIA/VLOA for "A" device, VHIB/VLOB for "B" device). The amplitude of the signal out of either Pin Driver device is approximately equal to VHI - VLO for that device (ie. VHIA - VLOA for the "A" device). The differential output of the Pin Driver drives the HLV308 output amplifier.

The HLV308 output amplifier is responsible for the amplitude and offset of the 9212 output signal. The amplitude is adjusted by varying the current to the ISINK pin. The current source on the HLV308 consists of a Gallium Arsenide (GaAs) FET in a common gate configuration. The purpose of this FET is to isolate the source node of the differential pair from PC board parasitics. The offset is adjusted by varying the voltage to the VOFFSET pin. The GaAs FET differential pair is driven such that all the ISINK current is switched. The purpose of the Drive Shaping circuit is to pre-distort the signal to the differential pair so that falling edge overshoot is suppressed. The Common Gate stage is biased by the voltage at the VCG pin and the currents to the ICGA and ICGB pins. The purpose of the Skin Effect Compensation circuit is to peak the signal out of the HLV308 to compensate for the skin effect of the output path of the 9212 (primarily due to the output relays).

4.2.2 9212 Functional Description (Block Diagram Figure 4-2)

The Pulse Shrink circuit receives the timing signal from the Mainframe and shrinks the pulse width depending on the state of the SHRINK* control signal. If SHRINK* is active (TTL "0") then pulse width out of the Pulse Shrink circuit is approximately 750ps less than the input pulse width. If SHRINK* is inactive (TTL "1") then the pulse shrink is 0. The output of the Pulse Shrink circuit is the input to the HLV308 hybrid.

The COMPLEMENT* control signal (TTL-level) is used to perform the INVERT function, which is selectable from the 9212 front panel. This is an active low signal (ie. INVERT occurs when COMPLEMENT* = Logic 0). The offset of the 9212 is adjusted by programming the OFFSET_DAC.

The amplitude of the 9212 is adjusted by first programming the ISINK_DAC. Then the amplitude of the drive signal to the HLV308 output amplifier is adjusted so that the GaAs FET differential pair fully switches. The amplitude of the drive signal is adjusted by

programming a coarse control (DRIVE_DAC) and a balance control (VHI_BAL_DAC). The VHI_BAL_DAC allows any offset errors between the pin driver outputs and differential pair FETs to be minimized. This is done by adjusting the VHI_BAL_DAC to minimize the difference voltage on the source node of the differential pair (the source node is accesible to the measurement system by means of the HLV308 VSM pin).

The transition time of the 9212 is adjusted by programming a coarse control (ERC_DAC) and a balance control (ERC_BAL_DAC). The balance control is used to minimize mismatch between the output rise time and fall time of the 9212.

The ICGA_DAC and ICGB_DAC are nominally programmed to half scale so that the common gate FETs are biased to approximately 17.5 mA. These DACs are programmable so that small median offset errors between the 9212 outputs may be nulled.

The Overvoltage Protection circuits protect both 9212 outputs from externally applied voltages. These circuits cause the Output Relays to open if greater than approximately 6 Volts is applied externally.

The Output Relays allow the 9212 outputs to be disabled (ie. - disconnected from the user's load). The OUT_EN control signal (TTL-level) is used to close the Output Relay for the 9212 normal output. The OUT*_EN control signal (TTL-level) is used to close the Output Relay for the 9212 complement output. Both OUT_EN and OUT*_EN are active high signals. The 9212 front panel DISABLE control opens both 9212 Output Relays. When in the disabled state, the outputs are both fed back to the Analog Multiplexer which programmably selects any one of its inputs to be connected to the Mainframe Voltage Readback. Furthermore, the 9212 normal output is fed back through the 6 dB 50 ohm Attenuator to the Mainframe Timing Readback. The Voltage Readback and Timing Readback allow the Mainframe to make the measurements it needs to auto calibrate the 9212 module.

4.3 General Description (Block Diagram Figure 4.3)

On the 9213, most of the signal path and signal fidelity determining functions are contained in the hybrid HSC309A and the surface mount amplifier 9213amp. The HSC309A is responsible for receiving the input timing signal, adjusting the transition time, fine amplitude control, signal inversion, a 10 db attenuator. The output of the HSC309A drives a 5 db attenuator and a pre-amp 20 db attenuator before being applied to the input of the 9213amp.

In general the signal is adjustable, via a DAC under microprocessor control, over a 5 db range (1.778:1). Therefore at 5 db increments throughout the range of amplitude operation an attenuator is switched into the signal path. This means there are 5 db, 10 db and two 20 db attenuators for a maximum attenuation of 55 db. The 5 db attenuator is comprised of surface mount components on the solder side of the PCB between the HSC309A and 9213amp and the 10 db attenuator is inside the HSC309A. There is a pre-amp 20 db attenuator and a post-amp 20 db attenuator. The reason for this is to optimize both signal-to-noise ratio at low amplitudes and transition time capability at low amplitudes. The attenuators are selected in the following order:

Required Attenuation	Attenuators Used
5 db	5 db
10 db	10 db
15 db	5 db & 10 db
20 db	pre-amp 20 db
25 db	pre-amp 20 db & 5 db
30 db	post-amp 20 db & 10 db
35 db	post-amp 20 db & 10 db & 5 db
40 db	both 20 db pre-amp + post-amp
45 db	pre-amp + post-amp 20 db + 5 db
50 db	pre-amp + post-amp 20 db + 10 db
55 db	pre-amp + post-amp 20 db, 10 db + 5 db

In order to maintain the full range of offset with the post-amp 20 db attenuator in place a separate offset voltage, atten_ofs, is generated and applied to the post-amp 20 db attenuator network when it is switched in.

The 9213amp is a composite current feedback amplifier. It is comprised of a wideband amplifier optimized for good pulse response but with relatively poor DC characteristics and a slower DC amplifier. The DC portion corrects the high frequency amplifier by comparing the output to the input and making the necessary corrections. Hence the term composite amplifier.

The remainder of the circuitry on the 9213 is output overvoltage and over-current protection and support circuitry (DACs and measurement circuitry) to provide control to the hybrid and amplifier.

A note of caution; since the system is auto calibrated it can be looked at as a closed loop system only during its calibration cycle. If there are any faults in the calibration feedback loops, strange behavior may result. As a result, care should be taken to verify all settings when troubleshooting. See section 6, TROUBLESHOOTING for more detailed information.

4.3.1 HSC309A (Block diagram Figure 4.1.1)

The HSC309A is comprised of the MSG305 (a custom designed IC), various capacitors and switches for different ranges of transition time programming, a complement switch and a 10 db attenuator. The entire signal path is differential.

A great deal of the functionality of the HSC309A is contained in the MSG305 as described below. The remainder of the HSC309A is comprised of emitter followers to buffer the MSG305 output and drive a PNP differential pair. The complement switch is implemented by either steering the output current from the differential pair straight through (normal) or cross-coupling the output current (inverted). The 10 db attenuator is a 50 ohm PI atttenuator network.

4.3.2 MSG305 (Block diagram Figure 4.1.2)

The purpose of the MSG305 is to accept the timing input and generate a signal with the requested rise and fall times. Additionally, the MSG305 is used to adjust the signal amplitude in small steps (<5 mV at the output) over a 5 db range. The MSG305 is capable of generating output rise and fall times as fast as 650 ps.

The operation of the MSG305 is reasonably straightforward. Timing inputs are accepted and conditioned to drive current switches. The currents that are switched are mirrored from input currents. These are the IRIN (I Rise IN) and IFIN (I Fall IN) inputs. The signal swings from VBOT to VTOP (which are nominally set at ± 538 mV) at a rate equal to the current divided by the equivalent capacitance. Since the current is variable over a large range (40 ua to 4 ma at the ICs internal node), the limiter employs a compensation scheme to cancel any variation in the limiting voltage as the current changes. There is a residual effect of about 10 - 20 mV that is measured and compensated for in firmware. The signal is buffered by a switchable input buffer whose input is a PNP emitter follower and applied to the output variable gain stage. A bias cancellation current (IINTZ) is input to cancel the PNP base current. This can vary from ≈20 uA to ≈120 uA from chip to chip. The output of the buffer is isolated by a large (4 kohm) resistor and sent off the chip as TSOUT. This signal is used as the comparison signal in the thermal tail compensation circuit as well as being used during calibration to eliminate chip to chip variations in offsets.

The MSG305 output stage is a current multiplying gain stage capable of gain variation over ≈2:1 range. It is a differential stage with the other input being AIN*. This input is used as the thermal compensation input. After a transition, the thermal effect is to cause the signal to increase in amplitude, usually with a long time constant. By applying a signal to AIN* and hence decreasing the input signal, the output signal amplitude is decreased.
Finally, a diode bridge switch is used to isolate the very high speed internal signal path from the external capacitors. This is so that the stray capacitance associated with the hybrid and additional capacitors does not slow down the very high speed edges. When the bridge is ON, the capacitors that exist in the HSC309 can be switched in to allow longer transition times to be programmed.

4.4 General Description (Block Diagram Figure 4.2)

Most of the 9214 functionality is implemented in the HLV308A hybrid. The HLV308A is responsible for adjusting the output amplitude and output offset. The Pulse Shrink circuit is responsible for decreasing ("shrinking") the minimum pulse width to under 1.2 ns. The rest of the 9214 is support circuitry for the HLV308A.

A note of caution; since the system is auto calibrated it can be looked at as a closed loop system only during its calibration cycle. If there are any faults in the calibration feedback loops, strange behavior may result. As a result, care should be taken to verify all settings when troubleshooting. See section 6, TROUBLESHOOTING for more detailed information.

4.4.1 HLV308 (Block Diagram Figure 4.2.1)

The HLV308A is comprised of an input differential pair, a level-shifting and reversing switch stage, the Pin Driver IC and the output amplifier. The entire signal path is differential. The input differential pair together with the level-shifting/reversing switch stage generates the input signal to the Pin Driver. The COMPLEMENT* control (TTL-level) is implemented by the reversing switch, and causes to be active either the Pin Driver normal input (COMPLEMENT* = Logic 1), or the Pin Driver complement input (COMPLEMENT* = Logic 0).

The Pin Driver is actually two separate devices on the same die. Each device has a differential input, edge rate control and single-ended output. In order to achieve a differential signal out of the Pin Driver, the two devices are used in a complementary fashion (ie. the "+" input of the "A" device is tied to the "-" input of the "B" device and vice versa). The Pin Driver is responsible for adjusting the amplitude of the drive signal to the HLV308A output amplifier. The amplitude of the signal out of the Pin Driver is adjusted by varying the VHI and VLO supplies. Each of the two Pin Driver devices has its own set of VHI and VLO supplies (VHIA/VLOA for "A" device, VHIB/VLOB for "B" device). The amplitude of the signal out of either Pin Driver device is approximately equal to VHI - VLO for that device (ie. VHIA - VLOA for the "A" device). The differential output of the Pin Driver drives the HLV308A output amplifier.

The HLV308A output amplifier is responsible for the amplitude and offset of the 9212 output signal. The amplitude is adjusted by varying the current to the ISINK pin. The current source on the HLV308A consists of a Gallium Arsenide (GaAs) FET in a common gate configuration. The purpose of this FET is to isolate the source node of the differential pair from PC board parasitics. The offset is adjusted by varying the voltage to the VOFFSET pin. The GaAs FET differential pair is driven such that all the ISINK current is switched. The purpose of the Drive Shaping circuit is to pre-distort the signal to the differential pair so that falling edge overshoot is suppressed. The Common Gate stage is biased by the voltage at the VCG pin and the currents to the ICGA and ICGB pins. The purpose of the Skin Effect Compensation circuit is to peak the signal out of the HLV308 to compensate for the skin effect of the output path of the 9214 (primarily due to the output relays).

4.4.2 9214 Functional Description (Block Diagram Figure 4-2)

The Pulse Shrink circuit receives the timing signal from the Mainframe and shrinks the pulse width depending on the state of the SHRINK* control signal. If SHRINK* is active (TTL "0") then pulse width out of the Pulse Shrink circuit is approximately 750ps less than the input pulse width. If SHRINK* is inactive (TTL "1") then the pulse shrink is 0. The output of the Pulse Shrink circuit is the input to the HLV308 hybrid.

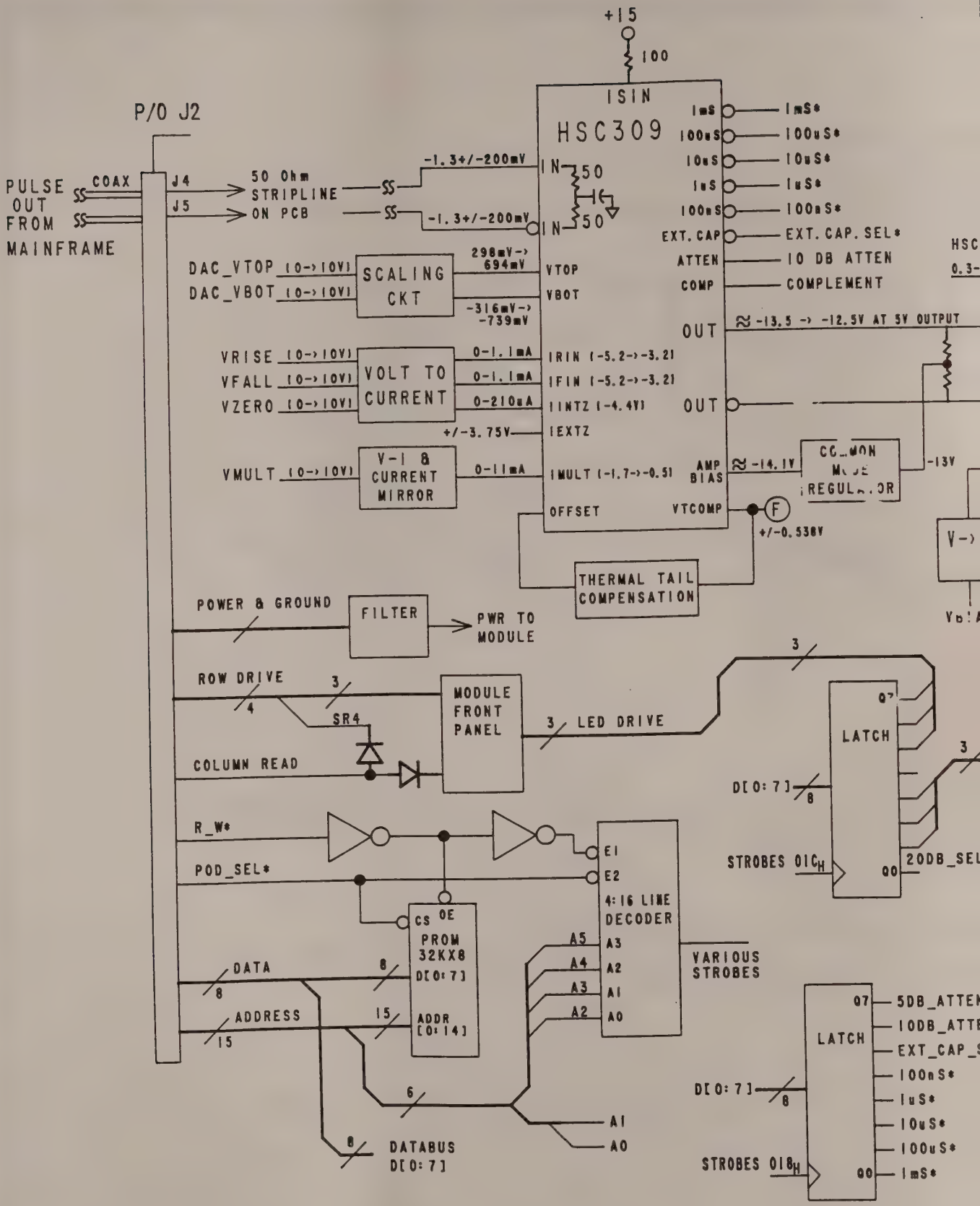
The COMPLEMENT* control signal (TTL-level) is used to perform the INVERT function, which is selectable from the 9214 front panel. This is an active low signal (ie. INVERT occurs when COMPLEMENT* = Logic 0). The offset of the 9214 is adjusted by programming the OFFSET_DAC.

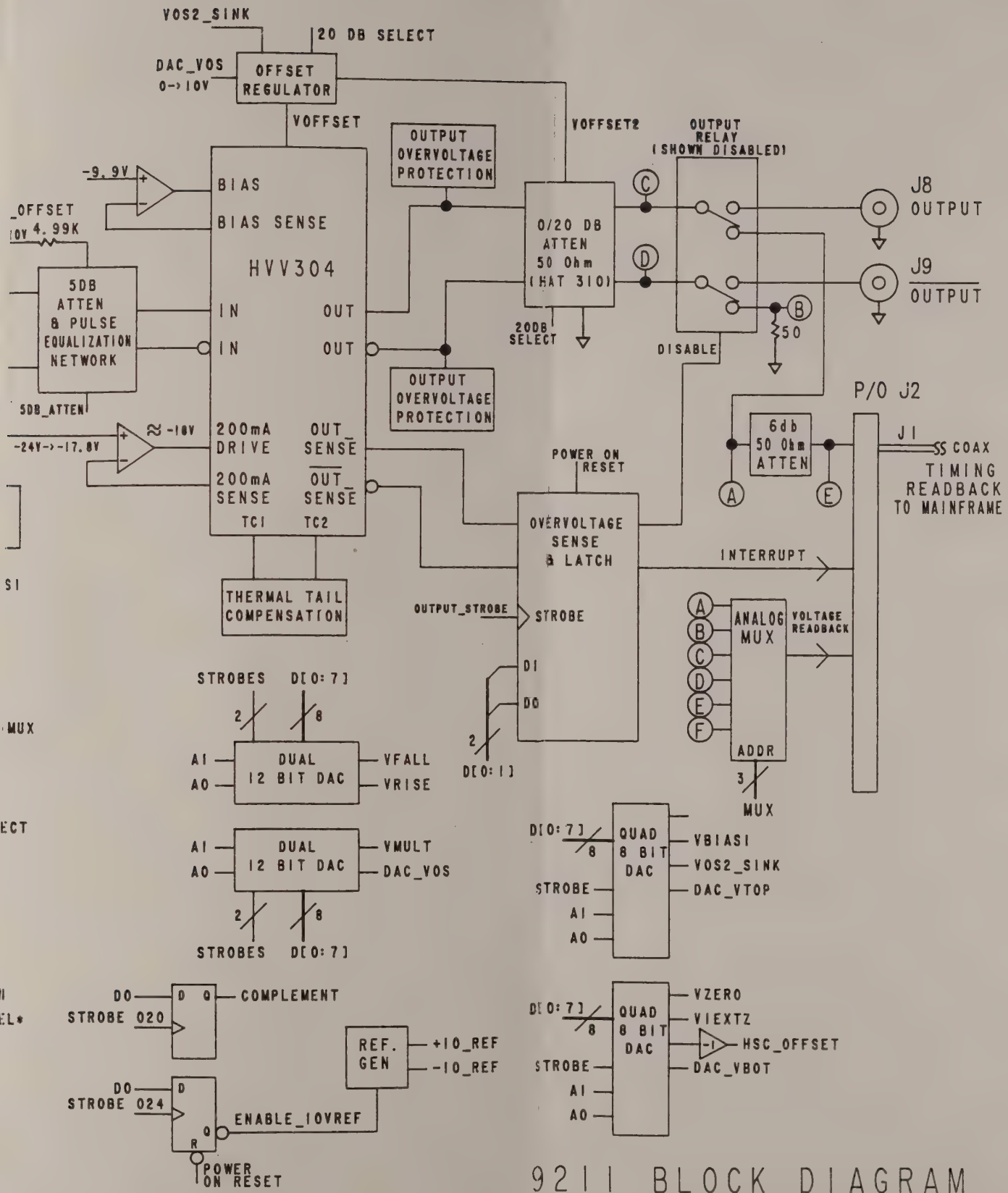
The amplitude of the 9214 is adjusted by first programming the ISINK_DAC. Then the amplitude of the drive signal to the HLV308A output amplifier is adjusted so that the GaAs FET differential pair fully switches. The amplitude of the drive signal is adjusted by programming a coarse control (DRIVE_DAC) and a balance control (VHI_BAL_DAC). The VHI_BAL_DAC allows any offset errors between the pin driver outputs and differential pair FETs to be minimized. This is done by adjusting the VHI_BAL_DAC to minimize the difference voltage on the source node of the differential pair (the source node is accesible to the measurement system by means of the HLV308 VSM pin).

The ICGA_DAC and ICGB_DAC are nominally programmed to half scale so that the common gate FETs are biased to approximately 17.5 mA. These DACs are programmable so that small median offset errors between the 9214 outputs may be nulled.

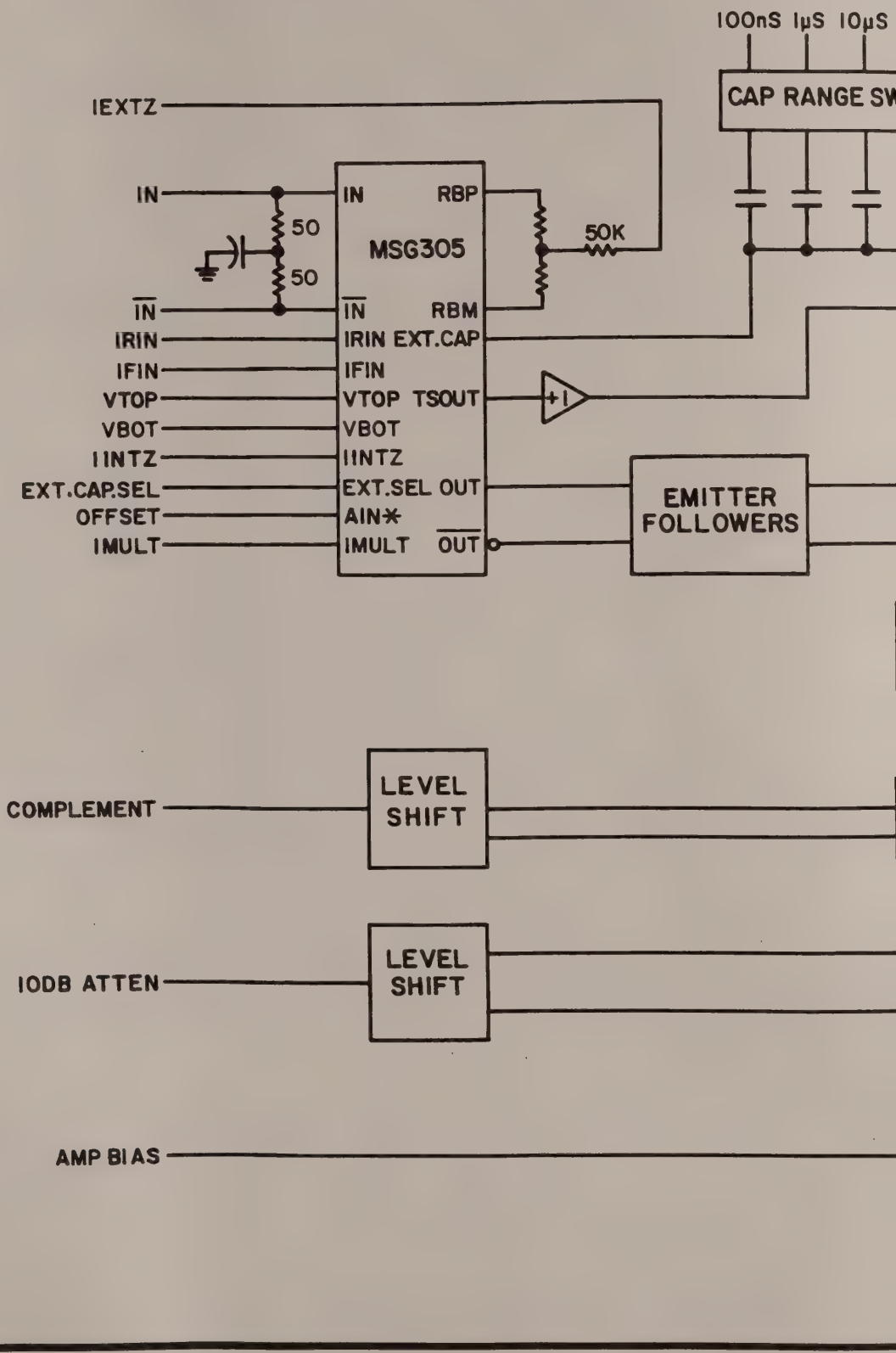
The Overvoltage Protection circuits protect both 9214 outputs from externally applied voltages. These circuits cause the Output Relays to open if greater than approximately 6 Volts is applied externally.

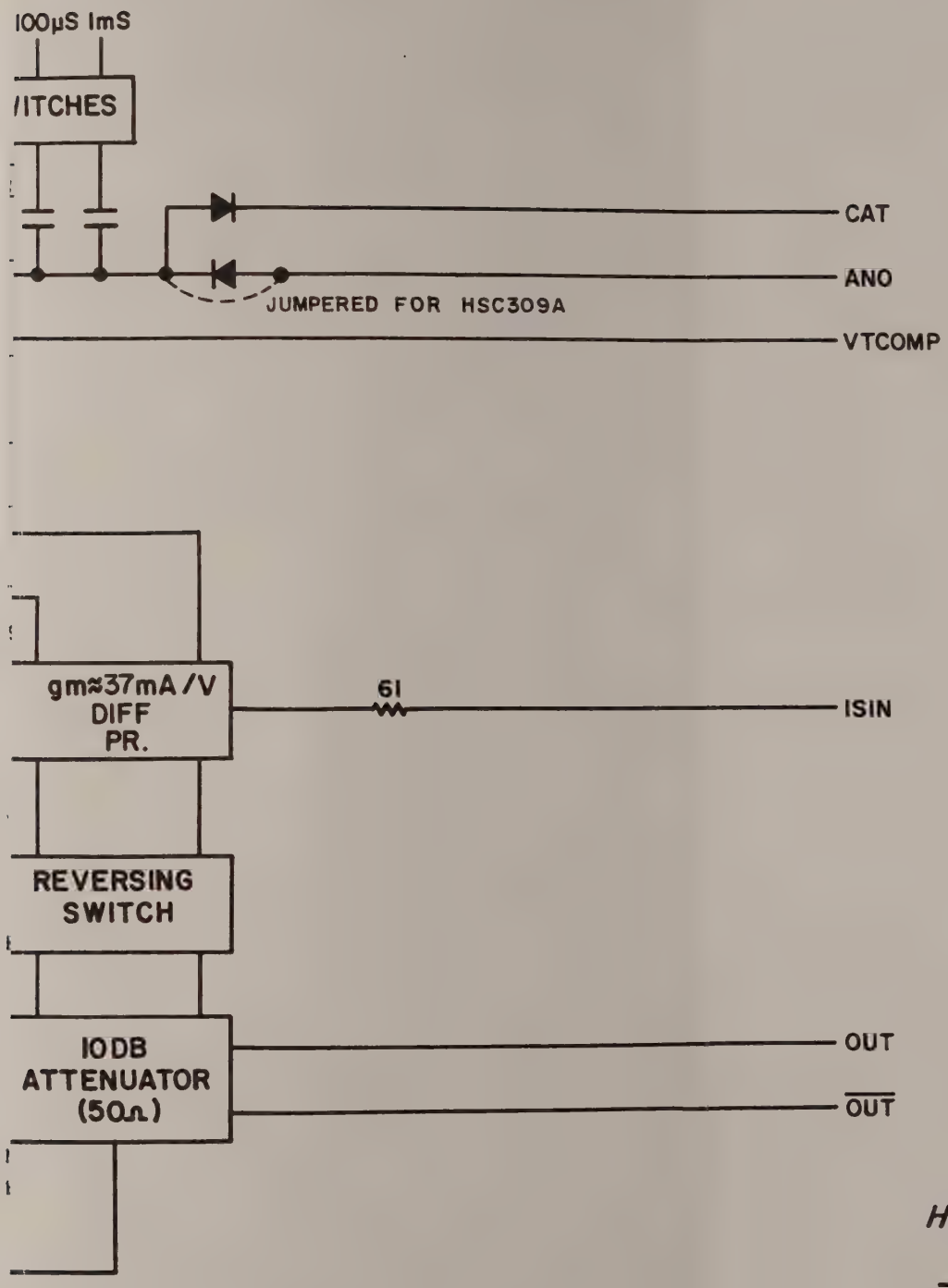
The Output Relays allow the 9214 outputs to be disabled (ie. - disconnected from the user's load). The OUT_EN control signal (TTL-level) is used to close the Output Relay for the 9214 normal output. The OUT*_EN control signal (TTL-level) is used to close the Output Relay for the 9214 complement output. Both OUT_EN and OUT*_EN are active high signals. The 9214 front panel DISABLE control opens both 9214 Output Relays. When in the disabled state, the outputs are both fed back to the Analog Multiplexer which programmably selects any one of its inputs to be connected to the Mainframe Voltage Readback. Furthermore, the 9214 normal output is fed back through the 6 dB 50 ohm Attenuator to the Mainframe Timing Readback. The Voltage Readback and Timing Readback allow the Mainframe to make the measurements it needs to auto calibrate the 9214 module.


+15
100
ISIN
HSC309
P/O J2
PULSE OUT FROM MAINFRAME
COAX
J4
J5
50 Ohm STRIPLINE ON PCB
-1.3+/-200mV
-1.3+/-200mV
IN 50
IN 50
1mS
100uS
10uS
1uS
100nS
EXT. CAP
ATTEN
COMP
1mS*
100uS*
10uS*
1uS*
100nS*
EXT. CAP. SEL*
10 DB ATTEN
COMPLEMENT
DAC_VTOP (0->10V)
DAC_VBOT (0->10V)
SCALING CKT
298mV-> 694mV
-316mV-> -739mV
VTOP
VBOT
OUT
≈ -13.5 -> -12.5V AT 5V OUTPUT
VRISE (0->10V)
VFALL (0->10V)
VZERO (0->10V)
VOLT TO CURRENT
0-1.1mA
0-1.1mA
0-210uA
IRIN (-5.2->-3.2)
IFIN (-5.2->-3.2)
IINTZ (-4.4V)
OUT
+/-3.75V
IEXTZ
VMULT (0->10V)
V-I & CURRENT MIRROR
0-11mA
IMULT (-1.7->-0.5)
AMP BIAS
≈ -14.1V
COMMON MODE REGULATOR
-13V
OFFSET
VTCOMP
F
+/-0.538V
THERMAL TAIL COMPENSATION
POWER & GROUND
FILTER
PWR TO MODULE
ROW DRIVE
SR4
COLUMN READ
MODULE FRONT PANEL
LED DRIVE
LATCH
D[0:7]
STROBES 01C_H
20DB_SEL
R_W*
POD_SEL*
E1
E2
4:16 LINE DECODER
VARIOUS STROBES
CS OE
PROM 32KX8
D[0:7]
ADDR [0:14]
DATA
ADDRESS
DATABUS D[0:7]
A5
A4
A3
A2
A3
A1
A0
A1
A0
LATCH
D[0:7]
STROBES 01B_H
5DB_ATTEN
10DB_ATTE
EXT_CAP_S
100nS*
1uS*
10uS*
100uS*
1mS*



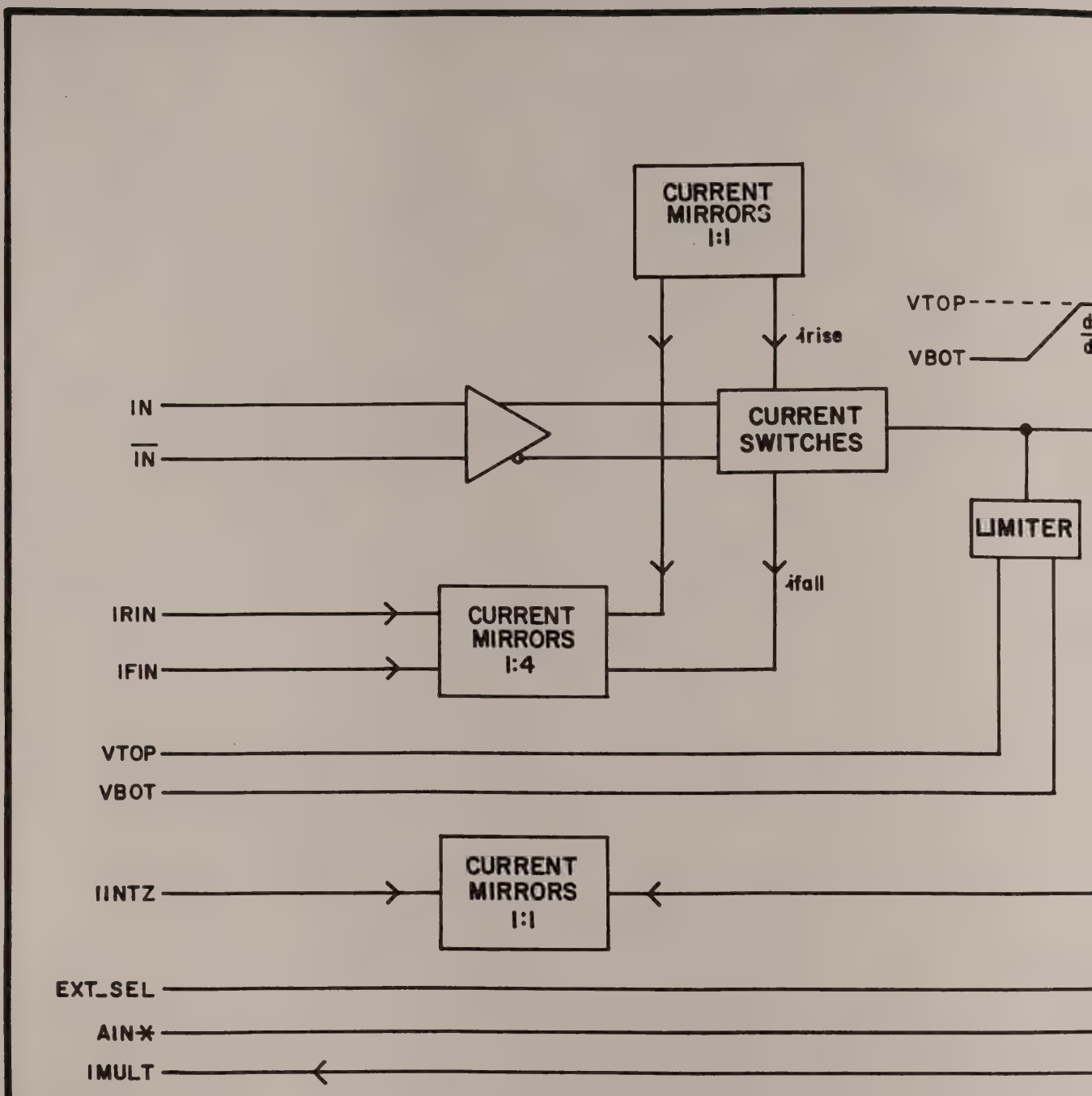
9211 BLOCK DIAGRAM
FIGURE 4-1

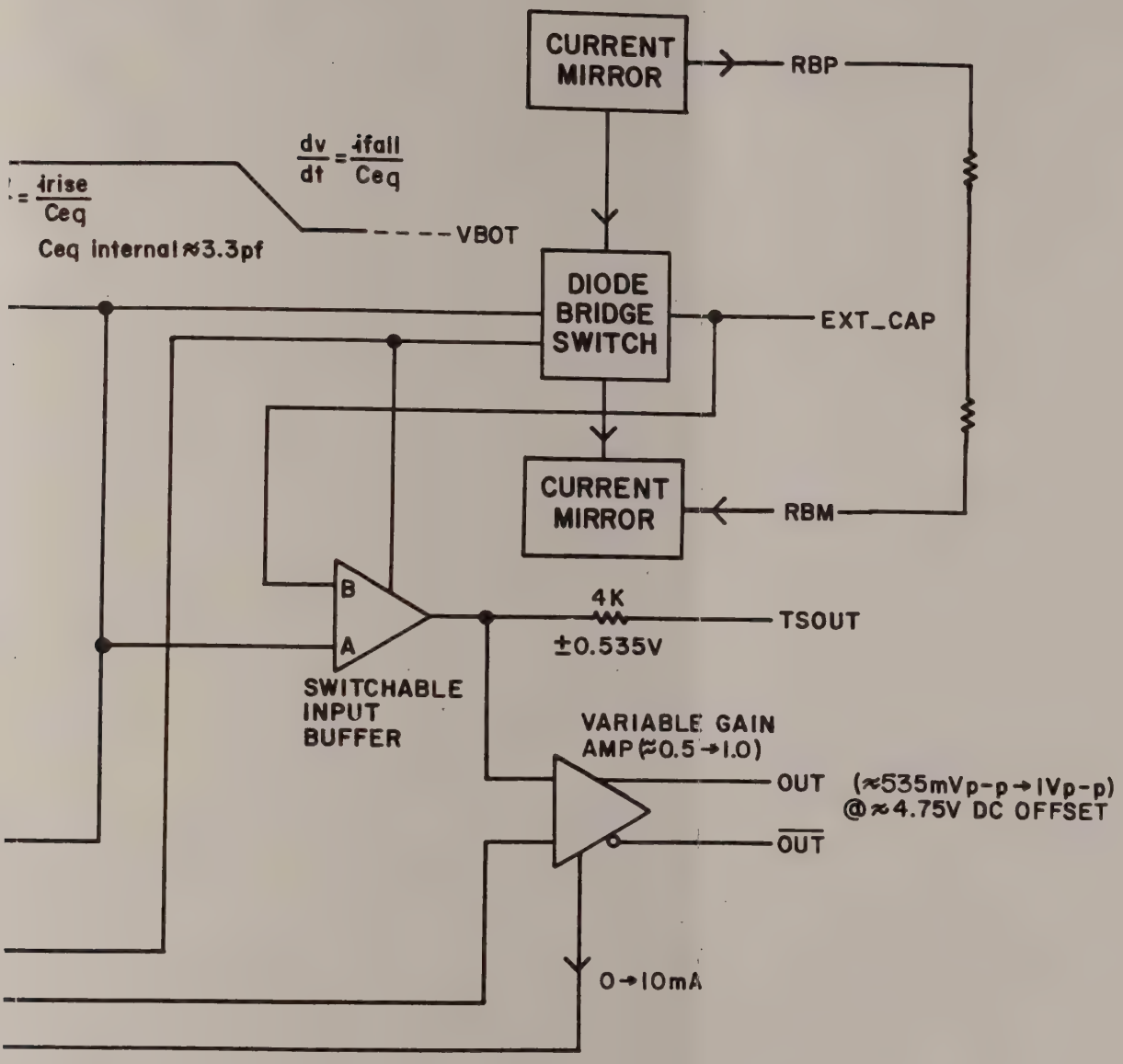

100nS
1μS
10μS
CAP RANGE SW
IEXTZ
IN
50
50
IN
IRIN
IFIN
VTOP
VBOT
IINTZ
EXT.CAP.SEL
OFFSET
IMULT
MSG305
IN
RBP
IN
RBM
IRIN EXT.CAP
IFIN
VTOP TSOUT
VBOT
IINTZ
EXT.SEL OUT
AIN*
IMULT
OUT
50K
+1
EMITTER FOLLOWERS
COMPLEMENT
LEVEL SHIFT
10DB ATTEN
LEVEL SHIFT
AMP BIAS



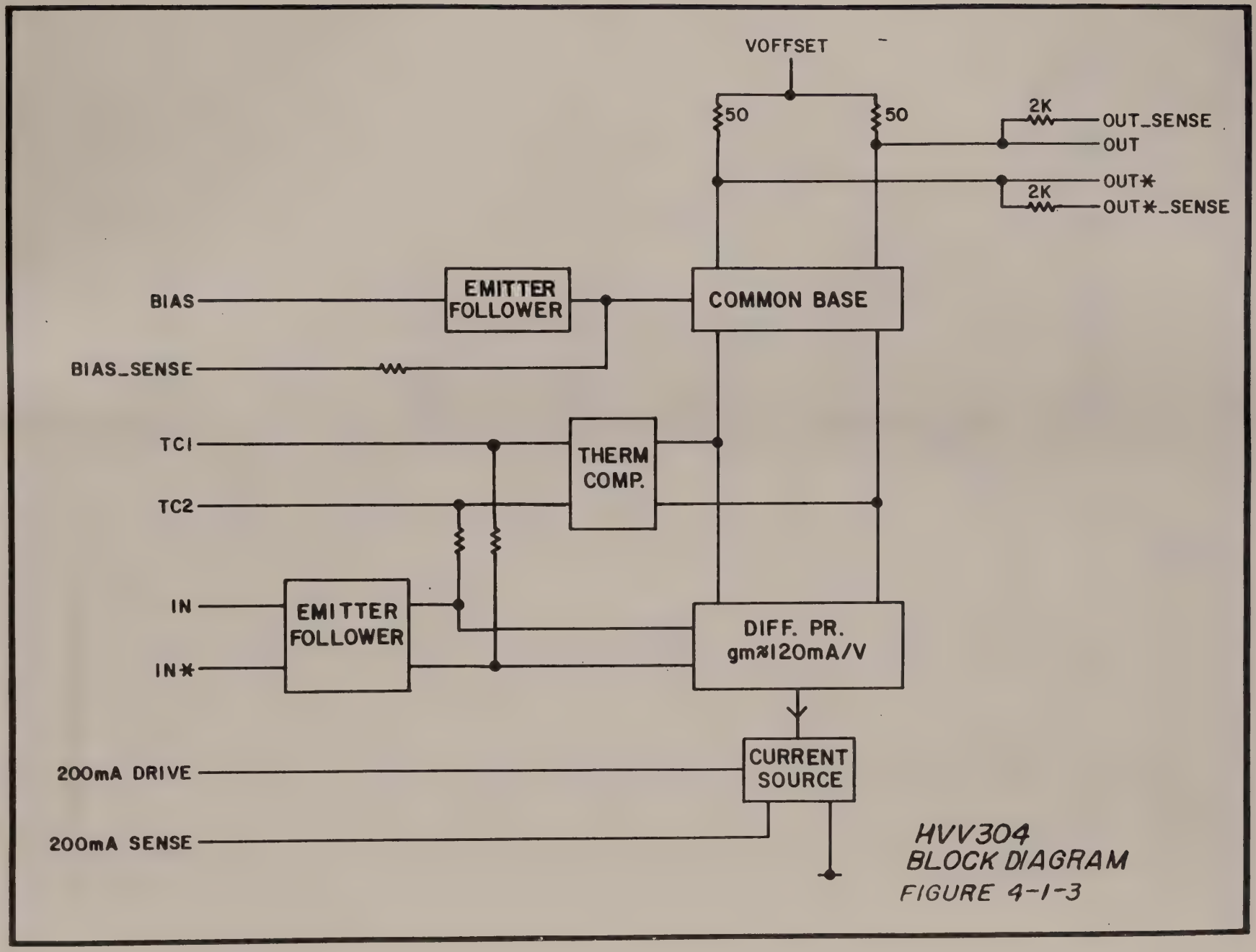
HSC309/HSC309A
BLOCK DIAGRAM

FIGURE 4-1-1

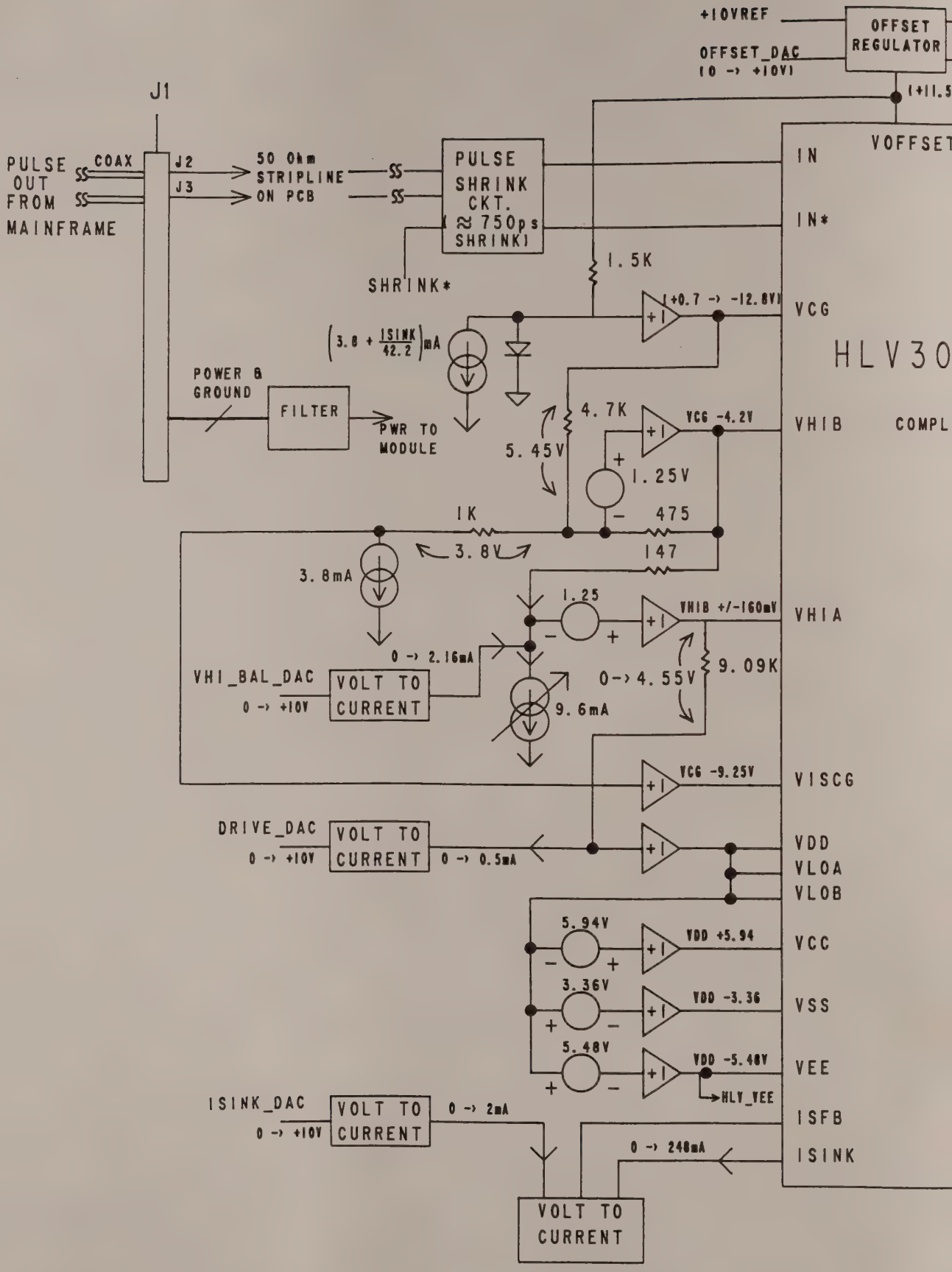

CURRENT MIRRORS 1:1
VTOP
VBOT
4rise
IN
$\overline{IN}$
CURRENT SWITCHES
LIMITER
4fall
IRIN
IFIN
CURRENT MIRRORS 1:4
VTOP
VBOT
IINTZ
CURRENT MIRRORS 1:1
EXT_SEL
AIN*
IMULT

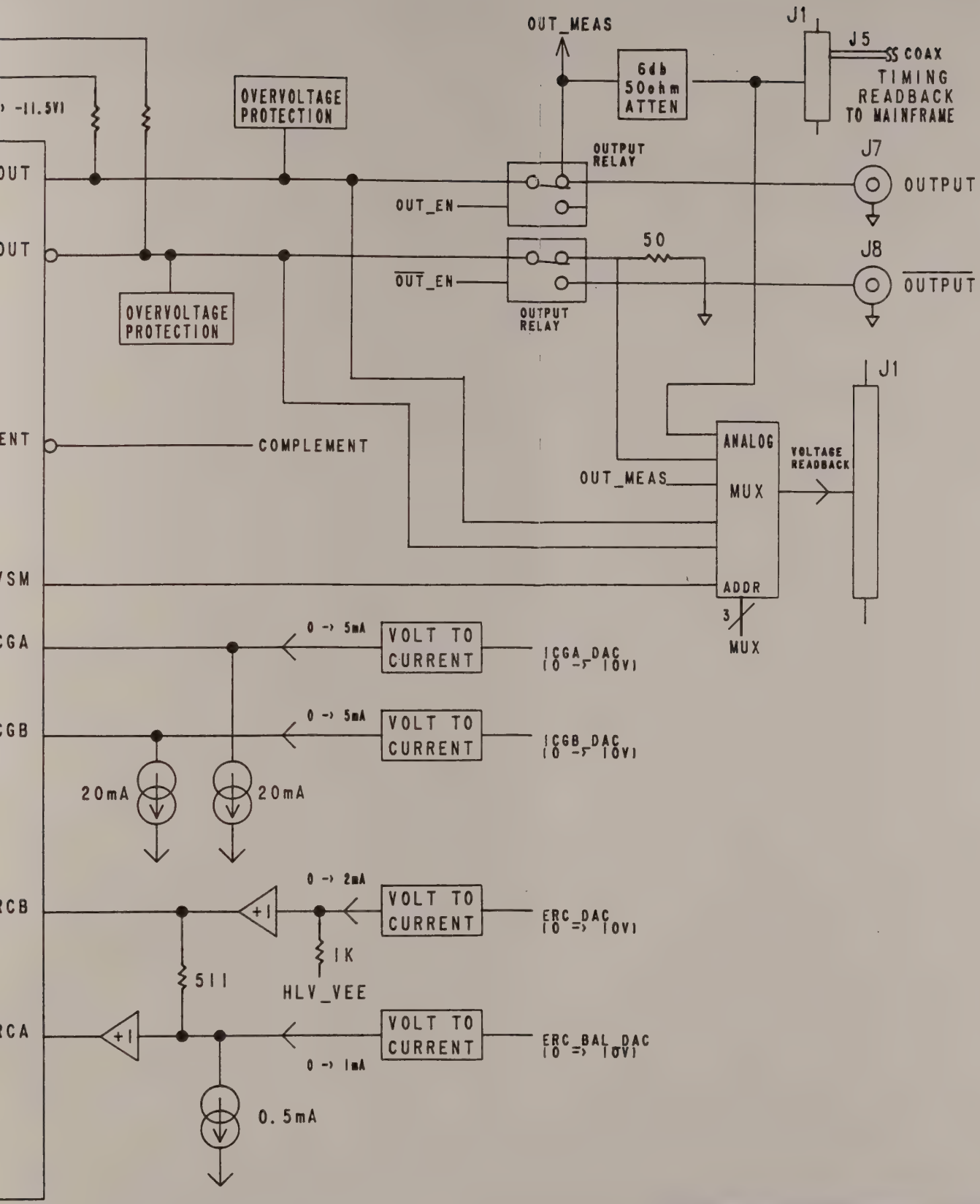


MSG305
BLOCK DIAGRAM
FIGURE 4-1-2



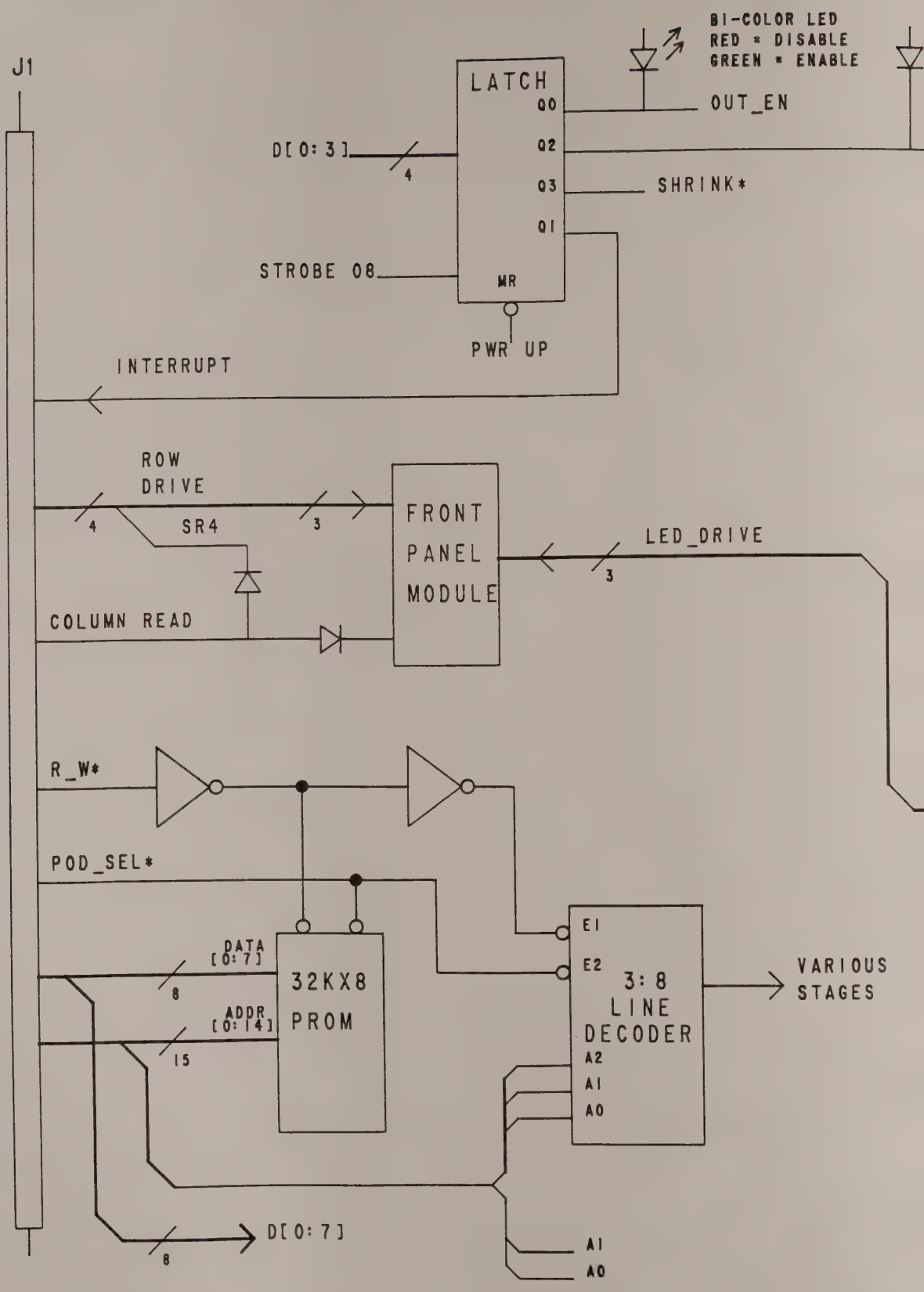
HVV304
BLOCK DIAGRAM
FIGURE 4-1-3

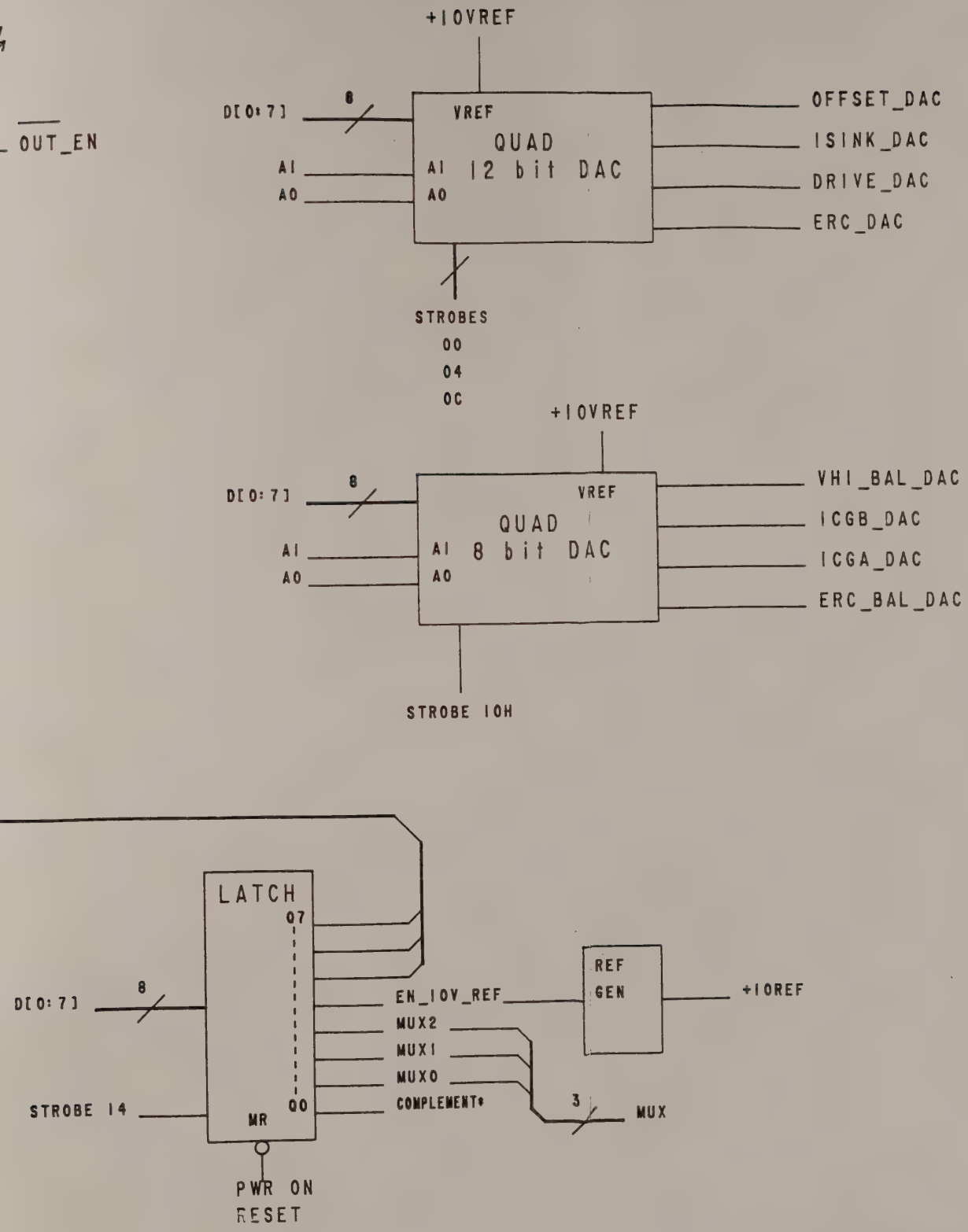

+10VREF
OFFSET REGULATOR
OFFSET_DAC
(0 -> +10V)
(+11.5
J1
PULSE OUT FROM MAINFRAME
COAX
J2
J3
50 Ohm STRIPLINE ON PCB
PULSE SHRINK CKT. (≈ 750ps SHRINK)
VOFFSET
IN
IN*
SHRINK*
1.5K
(+0.7 -> -12.8V)
VCG
(3.8 + ISINK/42.2)mA
HLV30
POWER & GROUND
FILTER
PWR TO MODULE
4.7K
VCG -4.2V
VHIB
COMPL
5.45V
1.25V
1K
475
3.8V
147
3.8mA
1.25
VHIB +/-160mV
VHIA
0 -> 2.16mA
VHI_BAL_DAC
0 -> +10V
VOLT TO CURRENT
0 -> 4.55V
9.09K
9.6mA
VCG -9.25V
VISCG
DRIVE_DAC
0 -> +10V
VOLT TO CURRENT
0 -> 0.5mA
VDD
VLOA
VLOB
5.94V
VDD +5.94
VCC
3.36V
VDD -3.36
VSS
5.48V
VDD -5.48V
VEE
HLV_VEE
ISINK_DAC
0 -> +10V
VOLT TO CURRENT
0 -> 2mA
ISFB
0 -> 248mA
ISINK
VOLT TO CURRENT



9212 and 9214 Block Diagram (1 of 2)

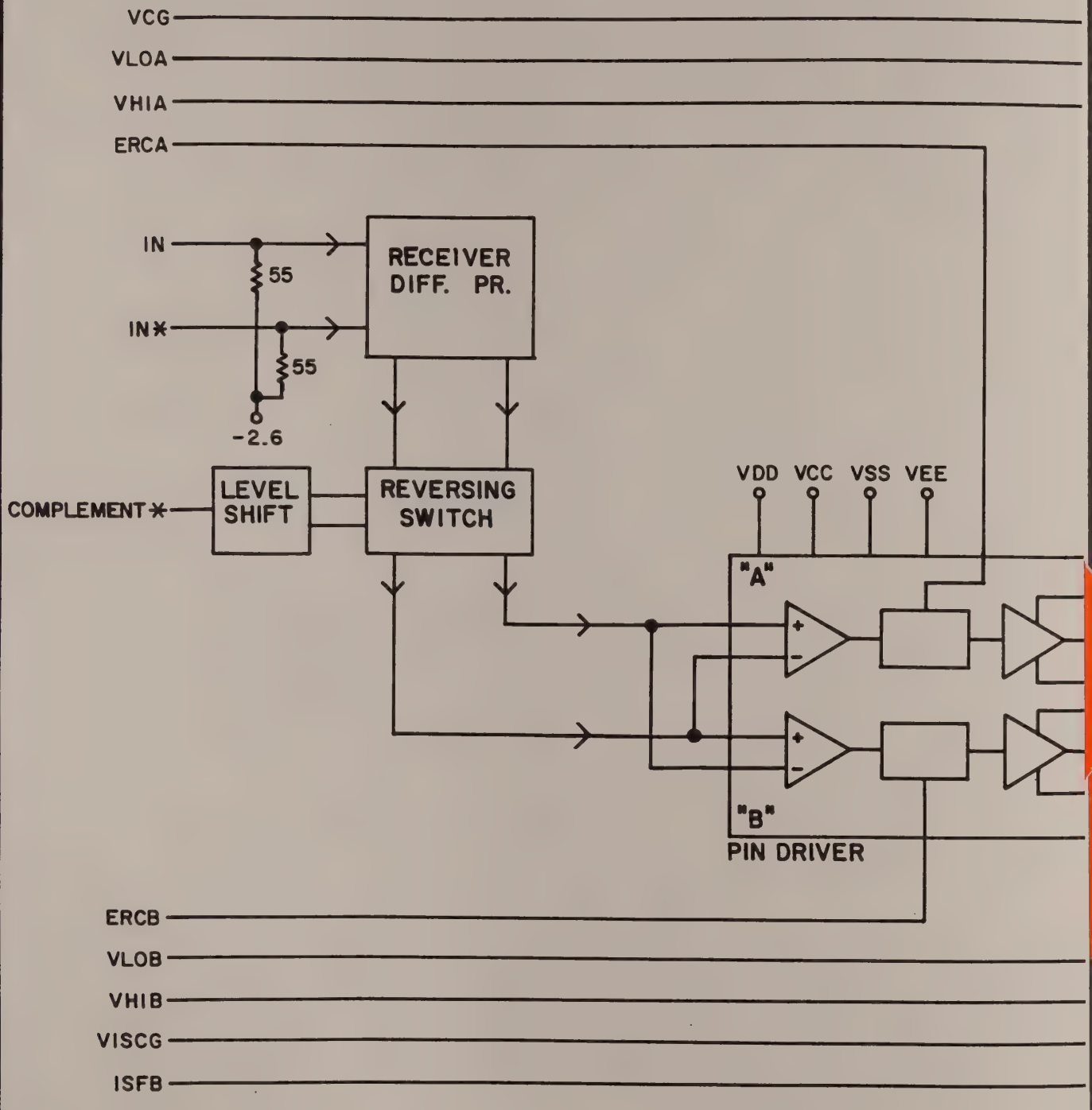
FIGURE 4-2

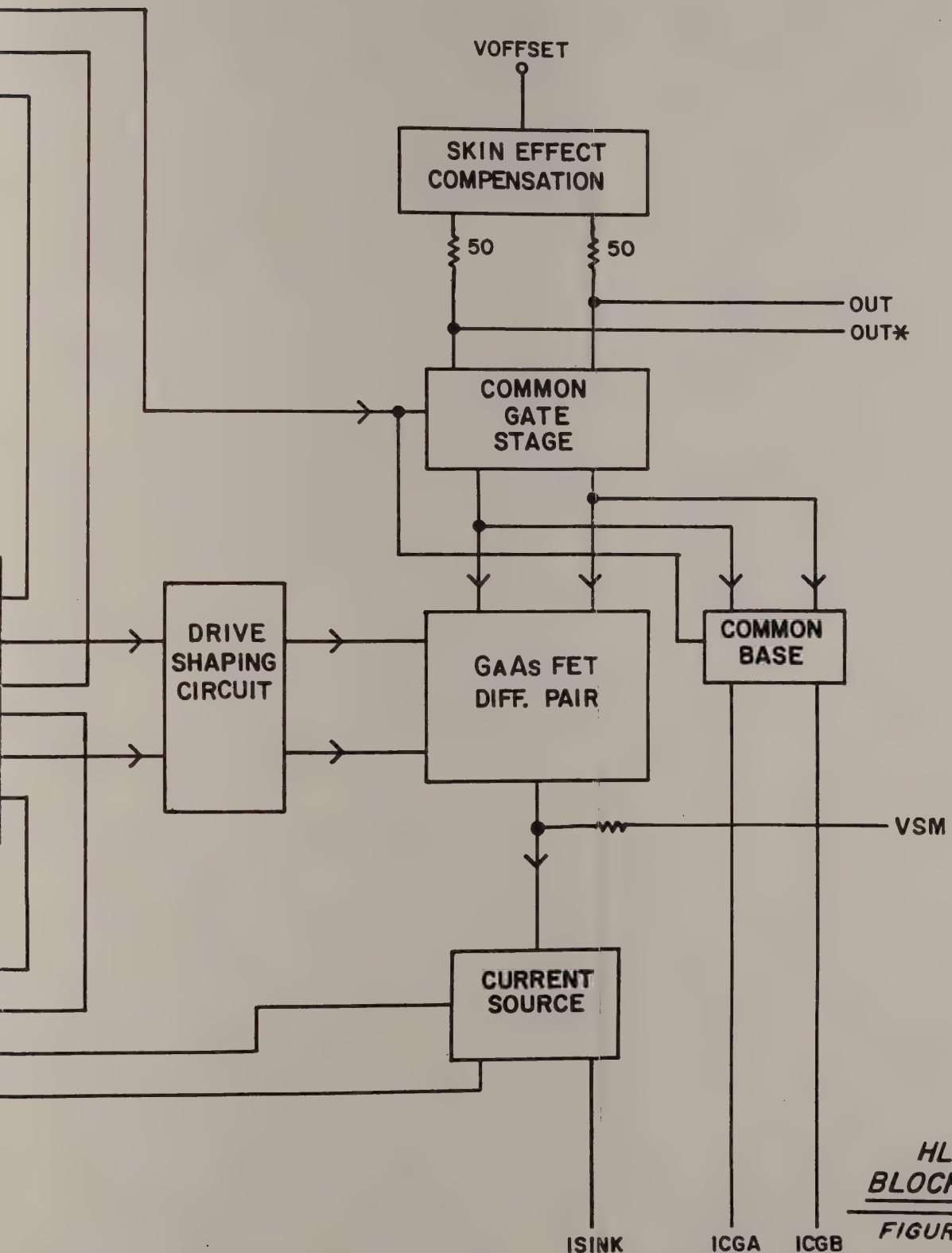

BI-COLOR LED
RED = DISABLE
GREEN = ENABLE
J1
LATCH
Q0
Q2
Q3
Q1
MR
OUT_EN
SHRINK*
D[0:3]
4
STROBE 08
PWR UP
INTERRUPT
ROW
DRIVE
4
SR4
3
FRONT
PANEL
MODULE
LED_DRIVE
3
COLUMN READ
R_W*
POD_SEL*
DATA
[0:7]
8
ADDR
[0:14]
15
32KX8
PROM
E1
E2
3:8
LINE
DECODER
A2
A1
A0
VARIOUS
STAGES
D[0:7]
8
A1
A0



9212 or 9214 Block Diagram (2 of 2)

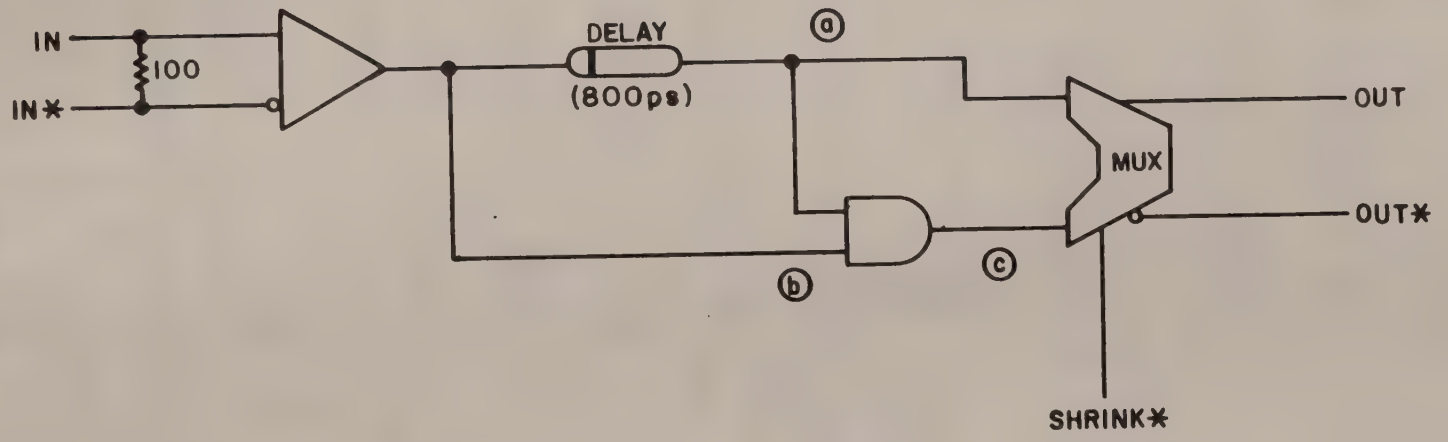
FIGURE 4-2 (CON'T)


VCG
VLOA
VHIA
ERCA
IN
IN*
55
55
-2.6
RECEIVER
DIFF. PR.
COMPLEMENT*
LEVEL
SHIFT
REVERSING
SWITCH
VDD
VCC
VSS
VEE
"A"
"B"
PIN DRIVER
ERCB
VLOB
VHIB
VISCG
ISFB

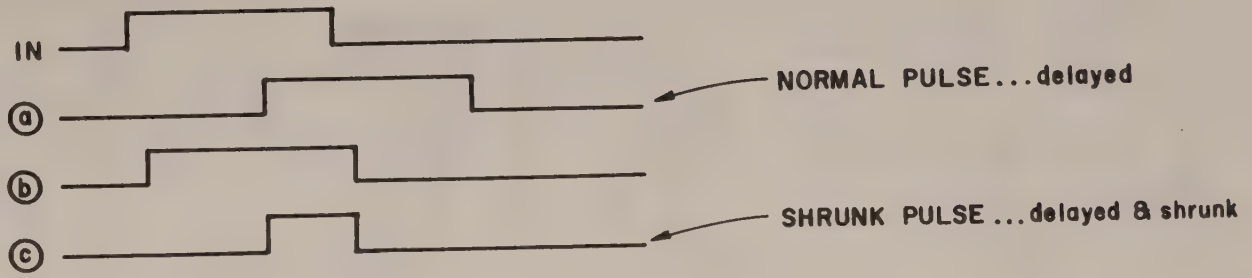


HLV308
BLOCK DIAGRAM

FIGURE 4-2-1

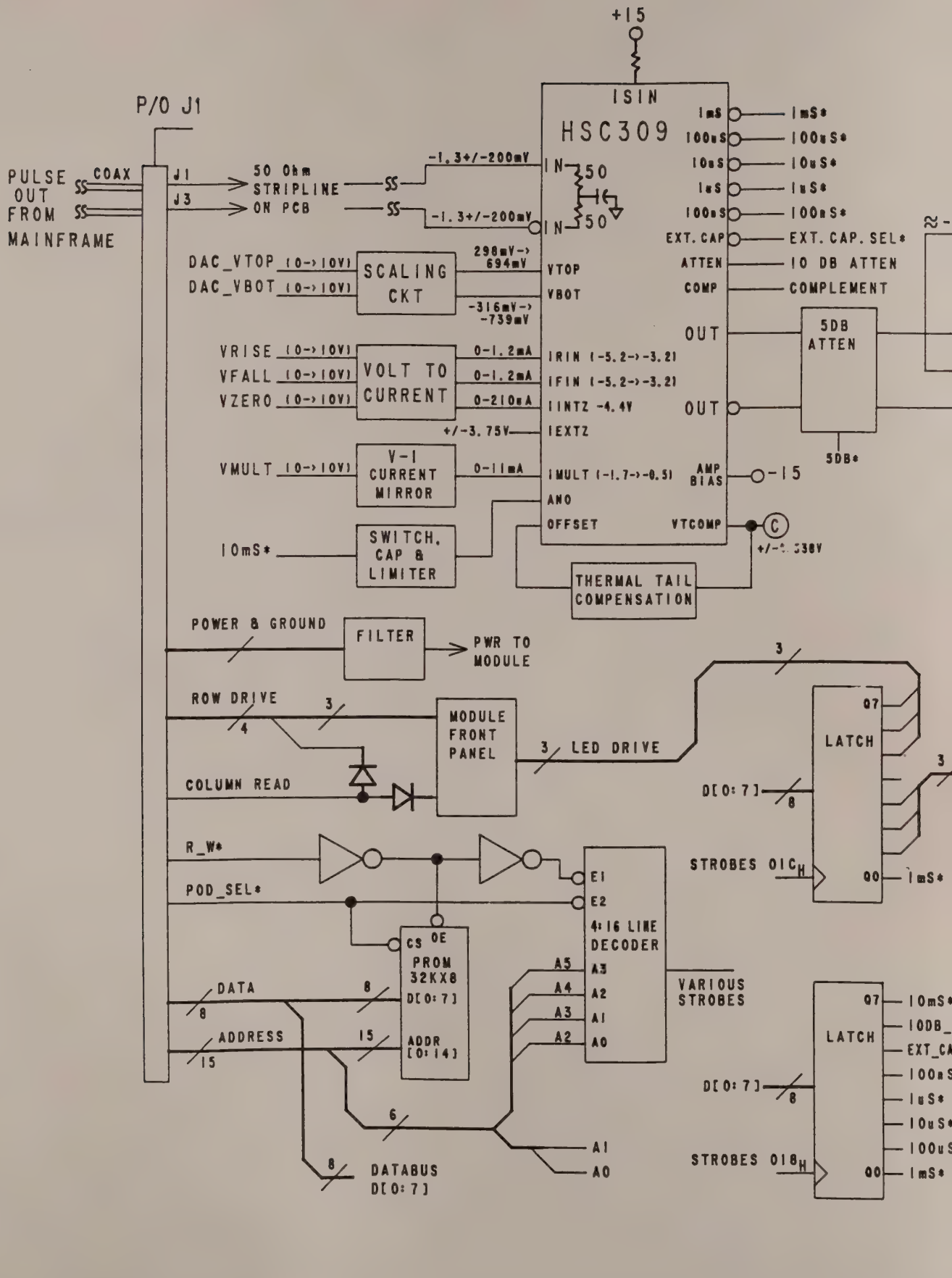


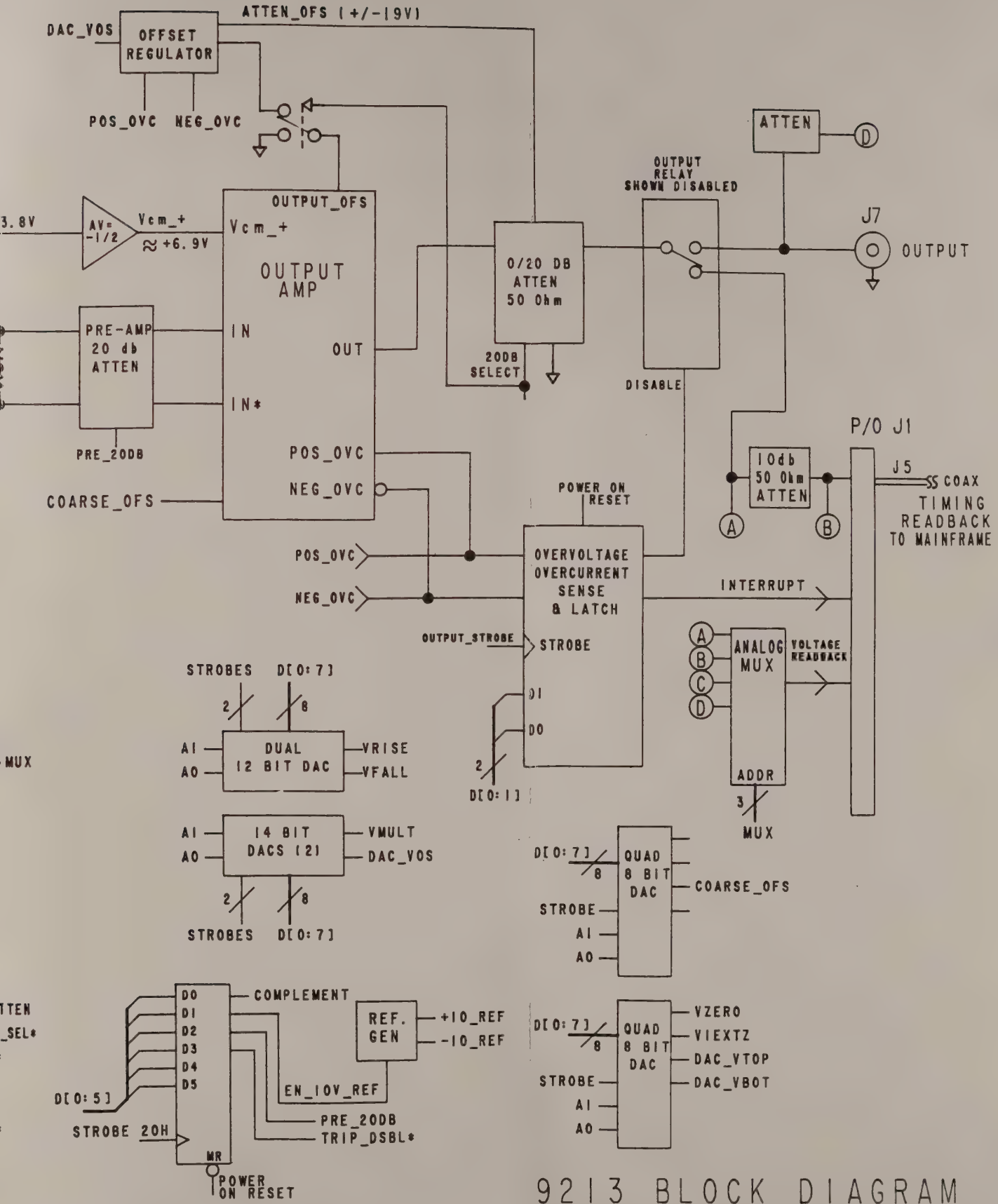
PULSE SHRINK TIMING



9212 PULSE SHRINKER

FIGURE 4-2-2


+15
ISIN
HSC309
P/O J1
PULSE OUT FROM MAINFRAME
COAX
J1
J3
50 Ohm STRIPLINE ON PCB
-1.3+/-200mV
IN
50
1mS
100uS
10uS
1uS
100nS
EXT. CAP
ATTEN
COMP
1mS*
100uS*
10uS*
1uS*
100nS*
EXT. CAP. SEL*
10 DB ATTEN
COMPLEMENT
DAC_VTOP (0->10V)
DAC_VBOT (0->10V)
SCALING CKT
298mV->694mV
-316mV->-739mV
VTOP
VBOT
OUT
5DB ATTEN
5DB*
VRISE (0->10V)
VFALL (0->10V)
VZERO (0->10V)
VOLT TO CURRENT
0-1.2mA
0-210uA
IRIN (-5.2->-3.2)
IFIN (-5.2->-3.2)
IINTZ -4.4V
+/-3.75V
IEXTZ
VMULT (0->10V)
V-I CURRENT MIRROR
0-11mA
IMULT (-1.7->-0.5)
AMP BIAS
-15
ANO
OFFSET
VTCOMP
10mS*
SWITCH, CAP & LIMITER
THERMAL TAIL COMPENSATION
POWER & GROUND
FILTER
PWR TO MODULE
ROW DRIVE
COLUMN READ
MODULE FRONT PANEL
LED DRIVE
LATCH
D[0:7]
STROBES 01C
R_W*
POD_SEL*
E1
E2
4:16 LINE DECODER
CS OE
PROM 32KX8
D[0:7]
ADDR [0:14]
DATA
ADDRESS
A5
A4
A3
A2
A1
A0
VARIOUS STROBES
STROBES 018
DATABUS D[0:7]



9213 BLOCK DIAGRAM
FIGURE 4-3

DISASSEMBLY

5.0 Introduction

This section includes the instruments disassembly and replacement procedures.

WARNING ***Anti-static protection measures should be taken prior to the handling of any printed circuit boards.***

5.1 PC Board

PC Board Removal

1. Power down the instrument and remove module.

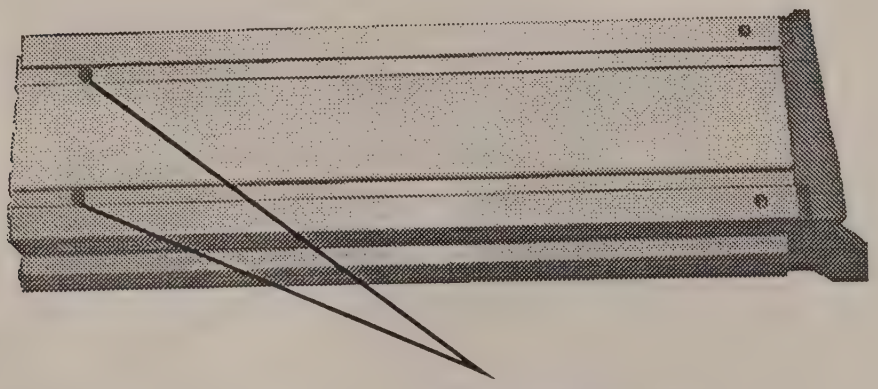
NOTE ***To remove the module from the instrument, lift the front edge (to clear locking device) and slide the unit forward.***

2. Remove the two screws from the rear of the module as shown in F M5.1.1

3. Remove the PC board from the rear of the module housing as shown in F M5.1.2

5.2 PC Board Replacement

1. Reverse the removal procedure to install the PC board.



(2) 4-40 Shoulder Screw
555-921-041

F M5.1.1 Module View (left side)

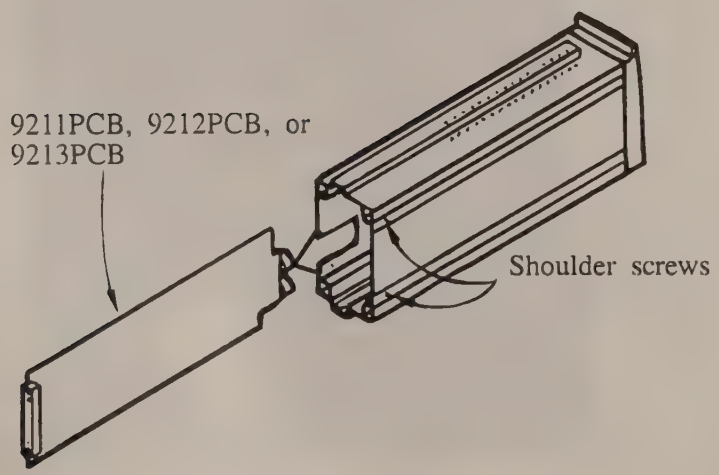
5.3 Module Front Panel PC Board

Front Panel PC Board Removal

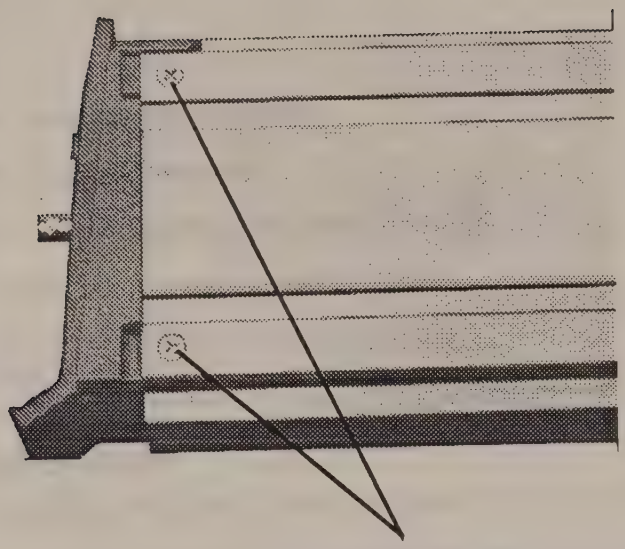
1. Perform the PC Board Removal procedure (Sect. 5.3).
2. Remove the two screws that attach the top and bottom guide rails to the module front panel as shown in F M5.3.1.
3. Remove the two side covers.
4. Depress the top guide rail locking tab and detach the rail from the front panel.
5. Depress the bottom guide rail locking tab and detach the rail from the front panel.
6. Remove the two screws that attach the module front panel PC board as shown in F M5.3.2.

Front Panel PC Board Replacement

1. Reverse the removal procedure to install the front panel PC board.

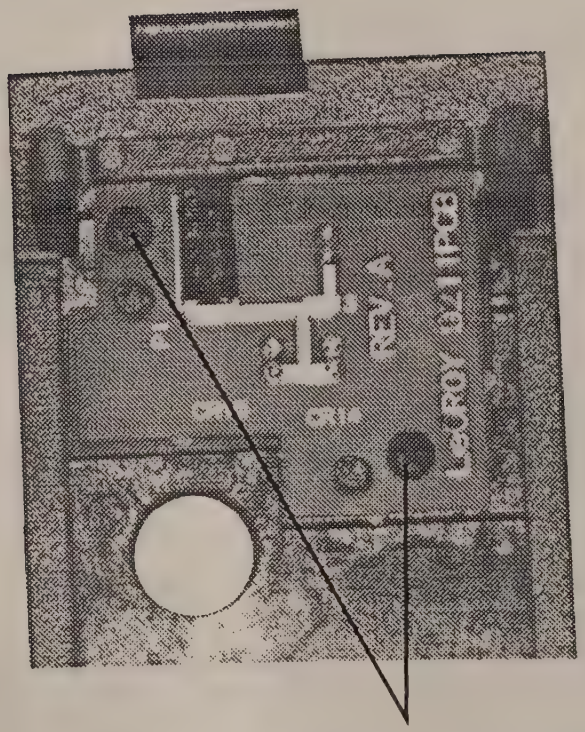


F M5.1.2 PC Board Removal



(2) Screw Flat Phil 6-32 x 5/16
567-632-005

F M5.3.1 Module View (right side)



(2) Screw self-tapping phil
555-511-005

F M5.3.2 Module Front Panel (rear view)

5.4 9213 Output Module Amplifier Board

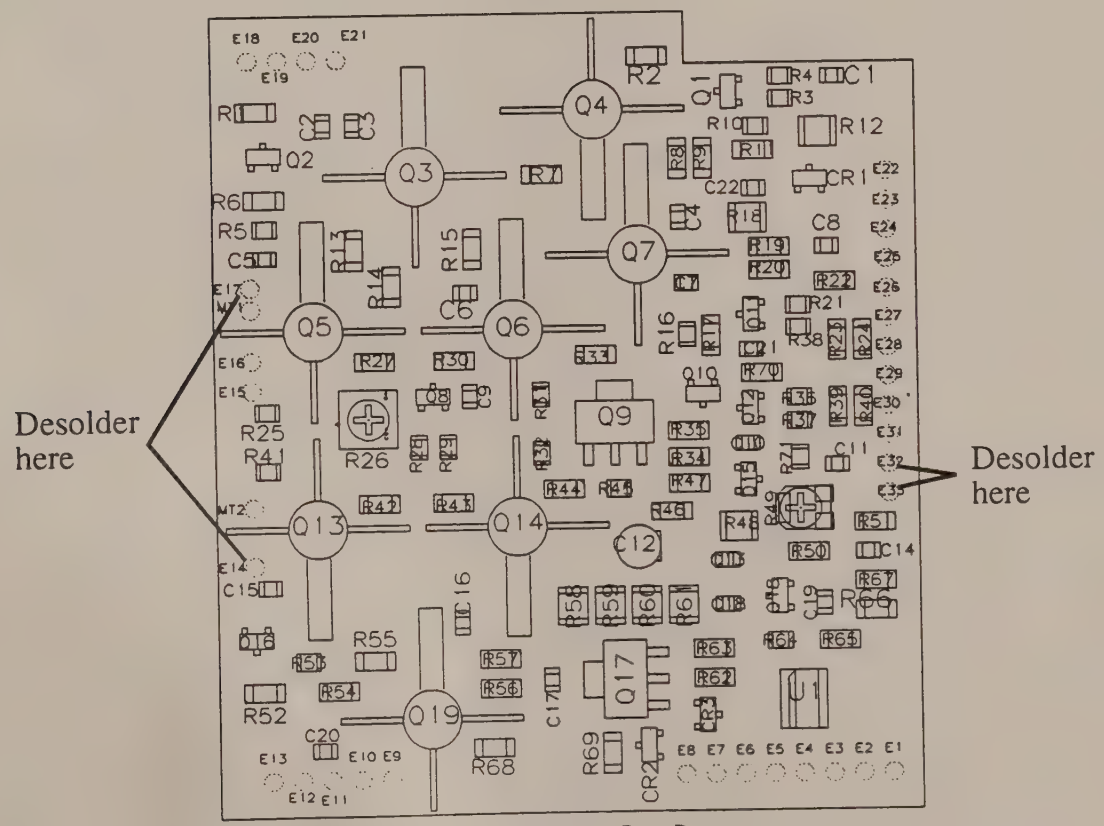
Amplifier PC Board (9213AMP) Removal

1. Perform the PC Board Removal procedure (Sect. 5.3).
2. Carefully desolder the locations shown in F M5.4.2.
3. Gently lift the Amplifier PC Board (9213AMP) off of the 9213 PC Board.

Amplifier PC Board Replacement

1. Reverse the removal procedure to install the Amplifier PC Board.

NOTE ***When reinstalling the Amplifier PC Board check that all pins are aligned with the respective locations on the 9213 PC Board.***



9213AMP Rev B.

F M5.4.1 9213AMP and PC Board Removal

92XX SERIES MODULE TROUBLESHOOTING

6.1 Introduction

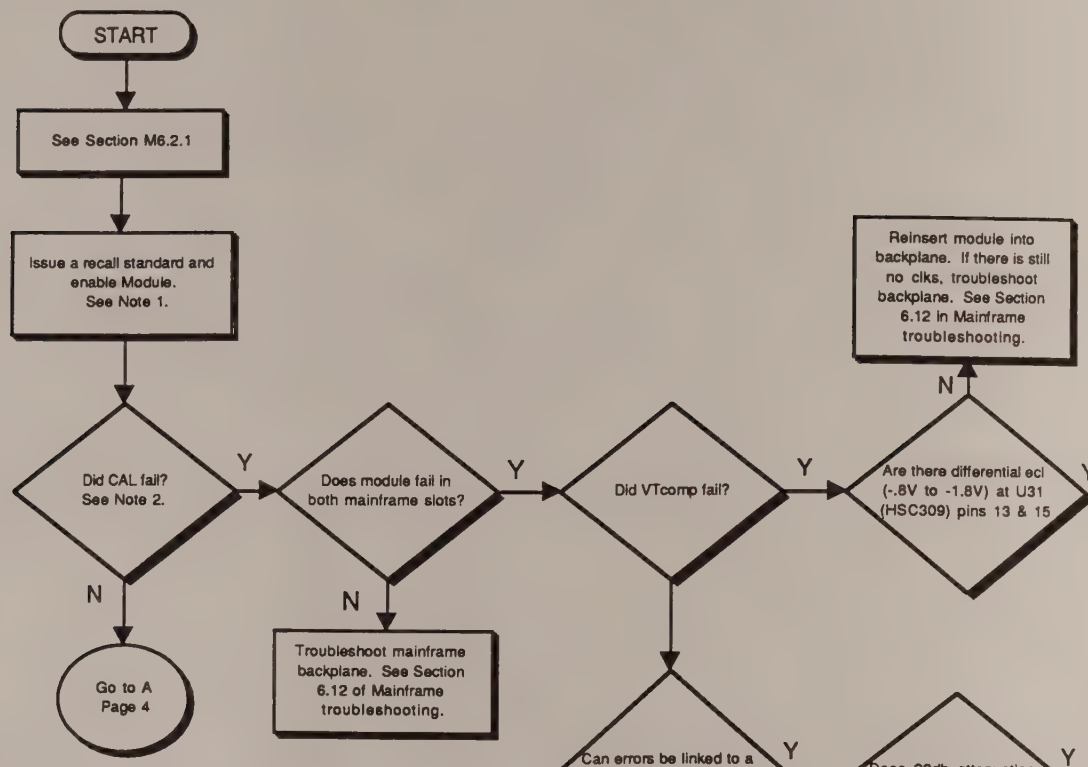
This section will guide service personnel in troubleshooting the 92XX series modules (9211,9212,9213), by the use of flow charts. The section is divided as follows:

1) 9211 MODULE
2) 9212 MODULE
3) 9213 MODULE
4) 9210 UTILITY PROGRAMS

When returning a part to the factory, please reference the malfunction code to customer service (where applicable).

A communication program is included in this manual to assist in troubleshooting the 92XX Modules as well as the 9210 Mainframe (see sec. 6.5). In order to troubleshoot certain module problems, the use of this program (or similar program) is required.

M6.2 9211 MODULE

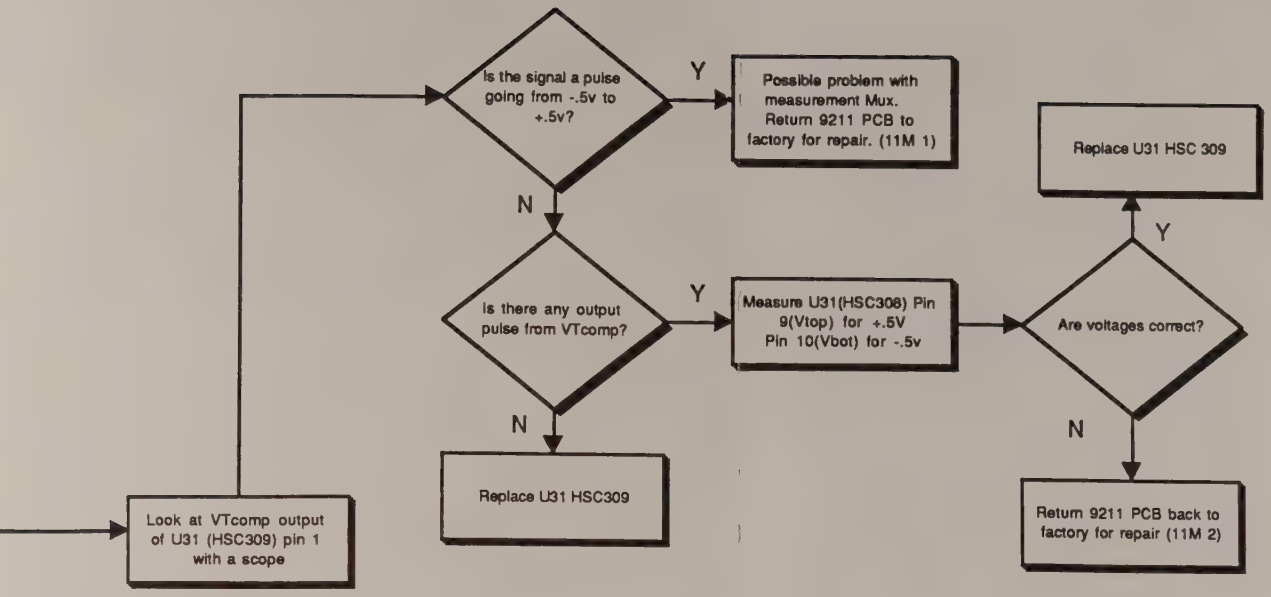


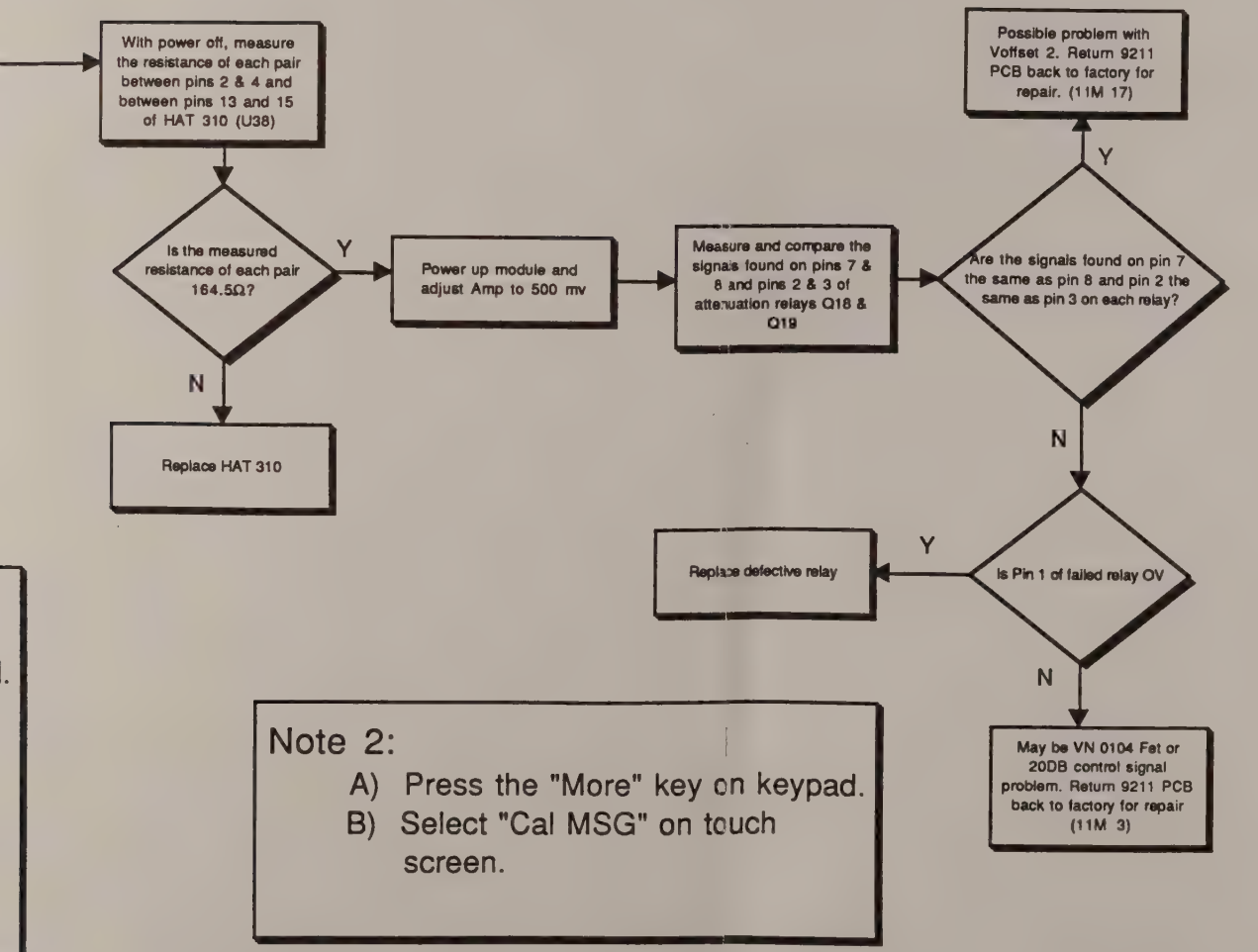
ATTENUATION CHART

Attenuation Stage	Attenuation Active
0db	None
5db	5db
10db	10db
15db	5db + 10db
20db	20db
25db	20db + 5db
30db	20db + 10db
35db	20db + 10db + 5db

Note 1:

A) Press the "More" key on keypa
B) Press the "Recall Setup" key o keypad.
C) Select "Standard" on the touch screen.
D) Press "Disable" key on Module keypad.

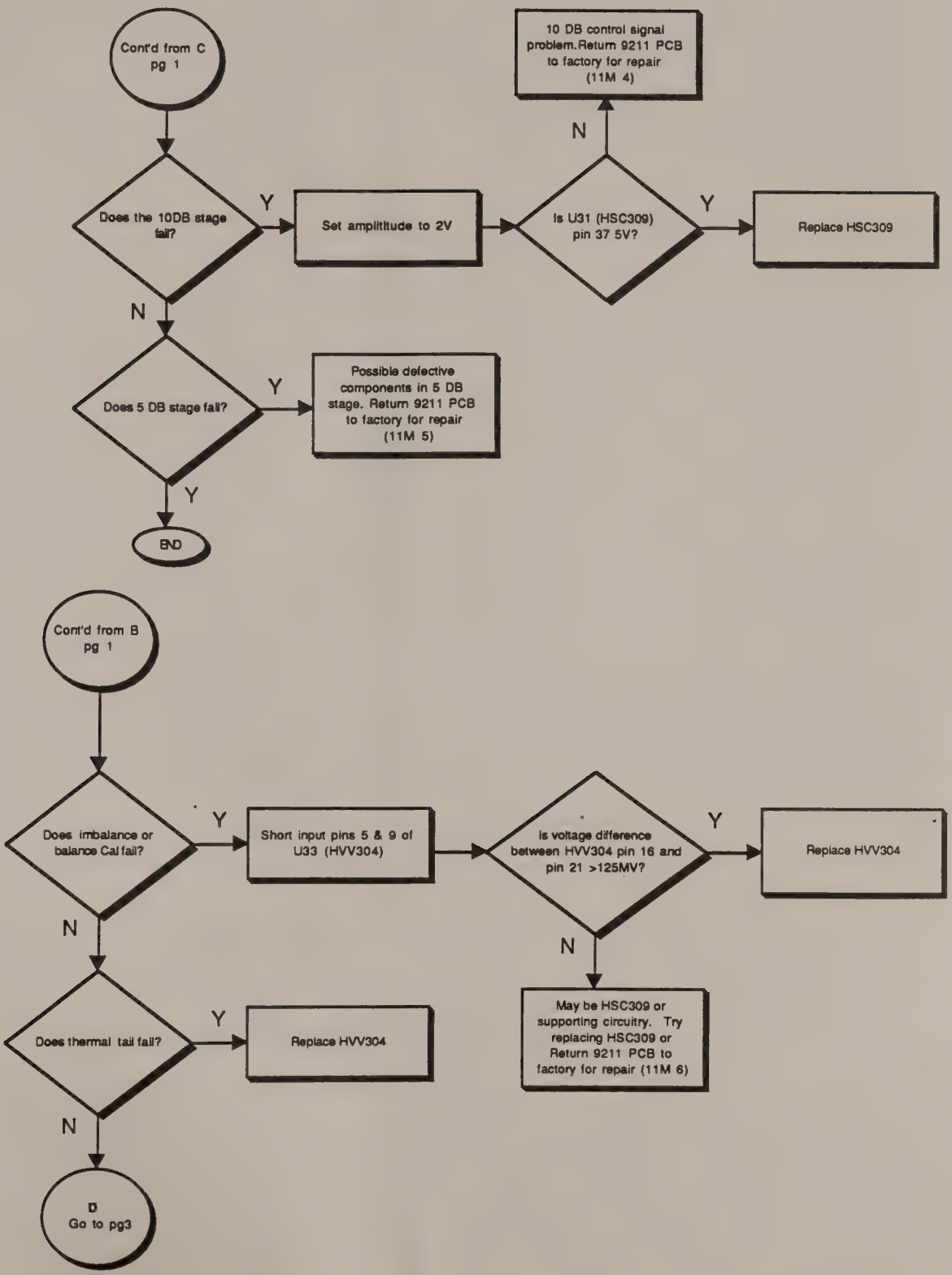


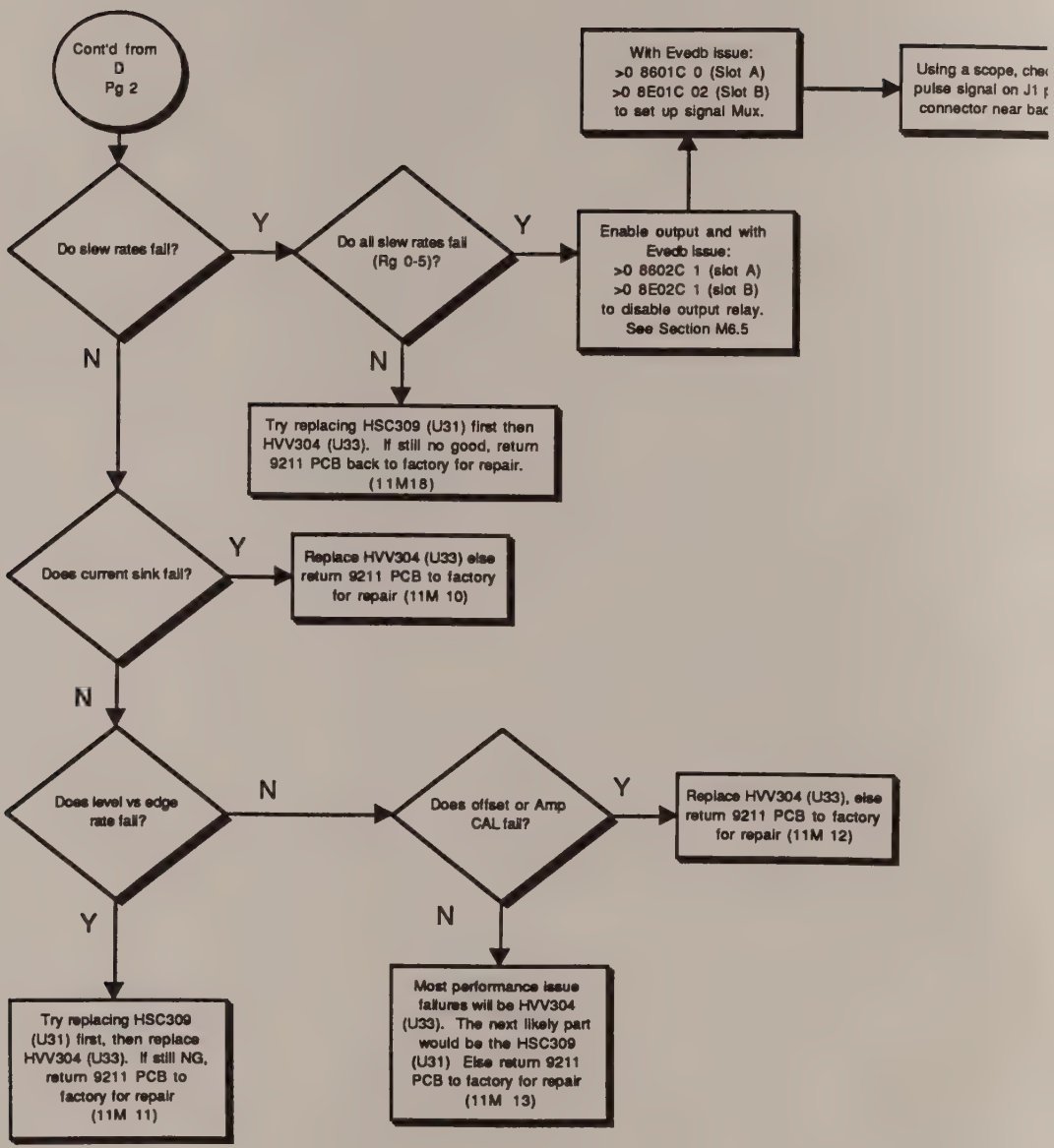


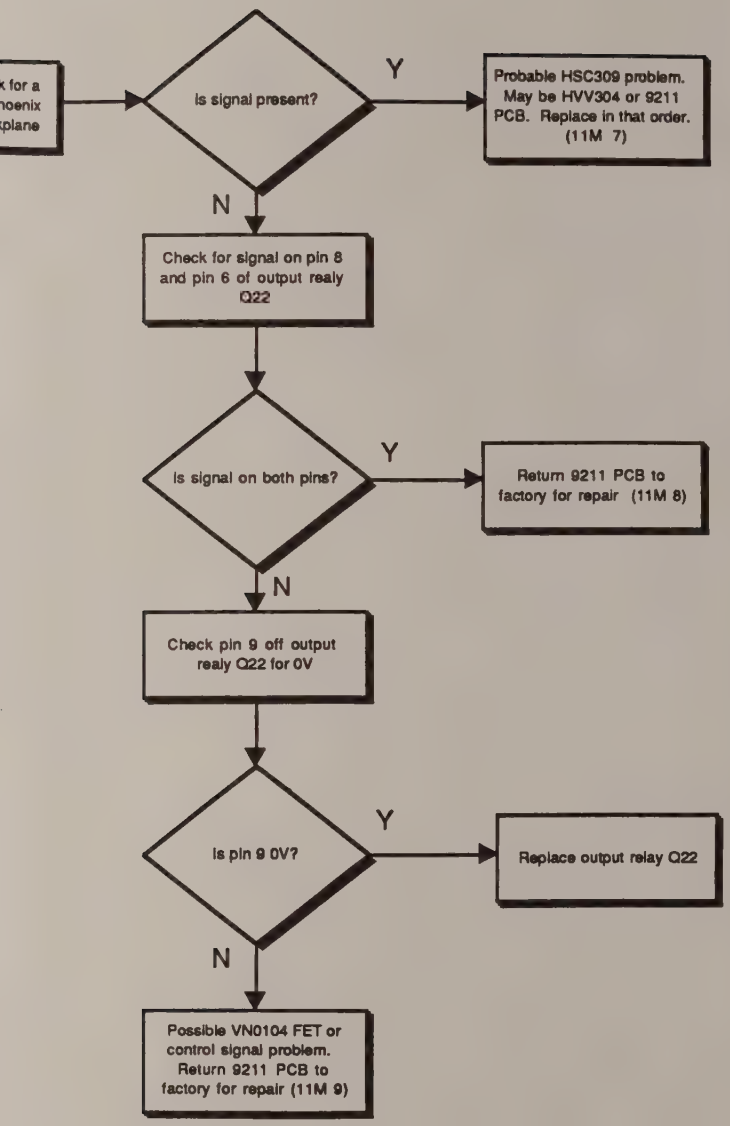
Note 2:

A) Press the "More" key on keypad.

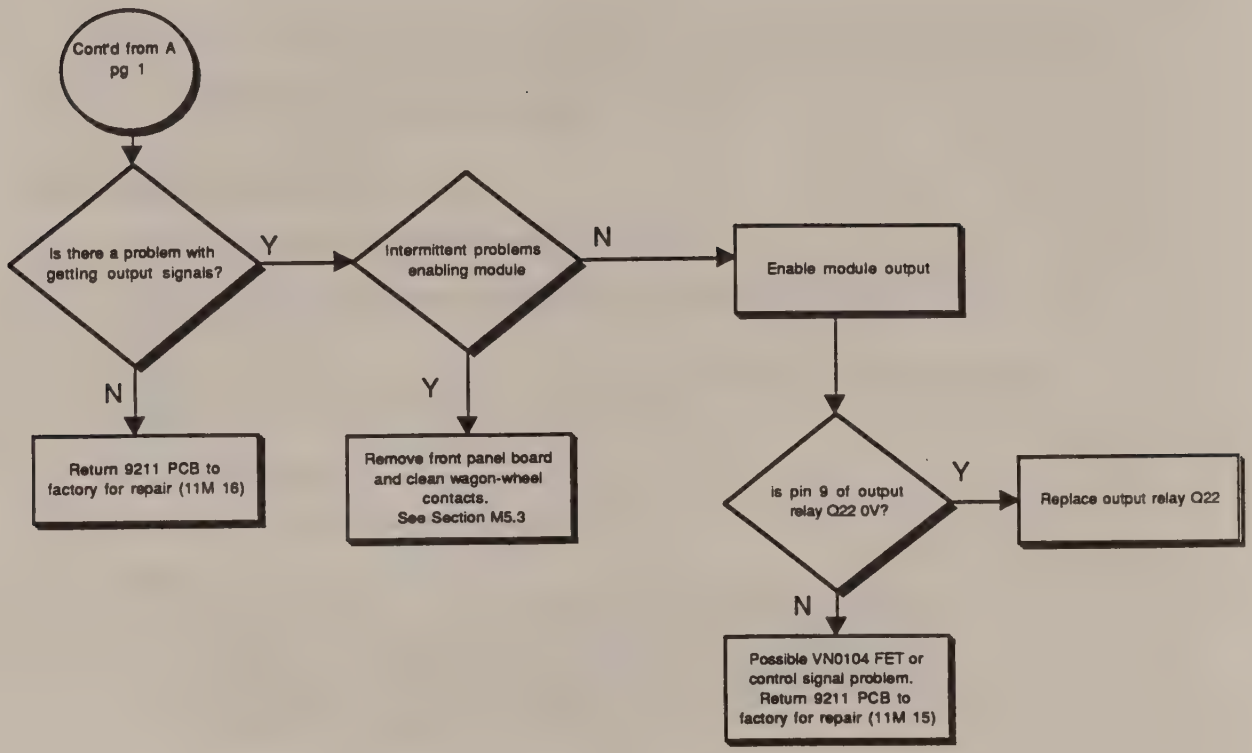
B) Select "Cal MSG" on touch screen.


Cont'd from C pg 1
Does the 10DB stage fail?
Y
Set amplitude to 2V
Is U31 (HSC309) pin 37 5V?
Y
Replace HSC309
N
10 DB control signal problem.Return 9211 PCB to factory for repair (11M 4)
N
Does 5 DB stage fail?
Y
Possible defective components in 5 DB stage. Return 9211 PCB to factory for repair (11M 5)
Y
END
Cont'd from B pg 1
Does imbalance or balance Cal fail?
Y
Short input pins 5 & 9 of U33 (HVV304)
Is voltage difference between HVV304 pin 16 and pin 21 >125MV?
Y
Replace HVV304
N
May be HSC309 or supporting circuitry. Try replacing HSC309 or Return 9211 PCB to factory for repair (11M 6)
N
Does thermal tail fail?
Y
Replace HVV304
N
D
Go to pg3


Cont'd from D Pg 2
Do slew rates fail?
Y
Do all slew rates fail (Rg 0-5)?
Y
With Evedb issue:
>0 8601C 0 (Slot A)
>0 8E01C 02 (Slot B)
to set up signal Mux.
Using a scope, che
pulse signal on J1
connector near bac
Enable output and with Evedb issue:
>0 8602C 1 (slot A)
>0 8E02C 1 (slot B)
to disable output relay.
See Section M6.5
N
N
Try replacing HSC309 (U31) first then HVV304 (U33). If still no good, return 9211 PCB back to factory for repair. (11M18)
Does current sink fail?
Y
Replace HVV304 (U33) else return 9211 PCB to factory for repair (11M 10)
N
Does level vs edge rate fail?
N
Does offset or Amp CAL fail?
Y
Replace HVV304 (U33), else return 9211 PCB to factory for repair (11M 12)
Y
N
Try replacing HSC309 (U31) first, then replace HVV304 (U33). If still NG, return 9211 PCB to factory for repair (11M 11)
Most performance issue failures will be HVV304 (U33). The next likely part would be the HSC309 (U31) Else return 9211 PCB to factory for repair (11M 13)


k for a
hoenix
xplane
Is signal present?
Y
Probable HSC309 problem. May be HVV304 or 9211 PCB. Replace in that order. (11M 7)
N
Check for signal on pin 8 and pin 6 of output realy Q22
Is signal on both pins?
Y
Return 9211 PCB to factory for repair (11M 8)
N
Check pin 9 off output realy Q22 for 0V
Is pin 9 0V?
Y
Replace output relay Q22
N
Possible VN0104 FET or control signal problem. Return 9211 PCB to factory for repair (11M 9)

M6.2 9211 MODULE
PAGE 4



6.2.1 9211 MODULE TROUBLESHOOTING

The troubleshooting tree should be used first in troubleshooting the module. Where a clear determination of the failure is not possible, further clarity may be attained by using the supplied Utilities Programs.

Due to the complexity of the 9211 circuitry, a control file (9211.CTL) is provided. The control file is downloaded to the 9210 Mainframe by using the program included on your Utilities Program Disk (see Sect. M6.5).

DOWNLOADING CONTROL FILE 9211.CTL

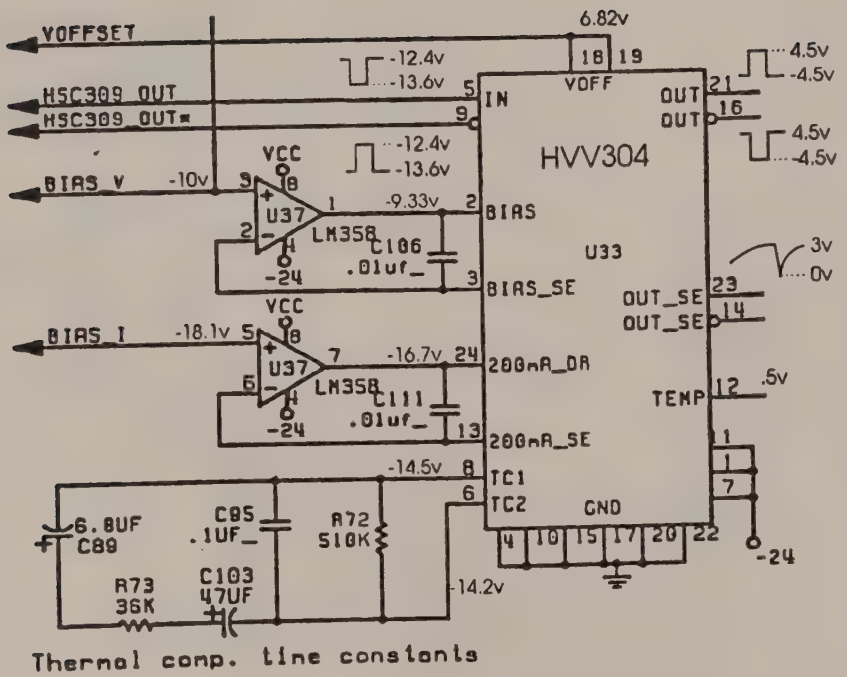
1. Install the supplied Utilities Disk (see Sect. M6.5).
2. Insert the 9211 Module into **CHANNEL B** of the 9210 Mainframe. Power on the mainframe.
3. Execute the EVEDB.EXE program (see Sect. M6.5) from the Utilities Program Disk.
4. Issue the following:

   COMMAND>**F 9211.CTL**

   NOTE

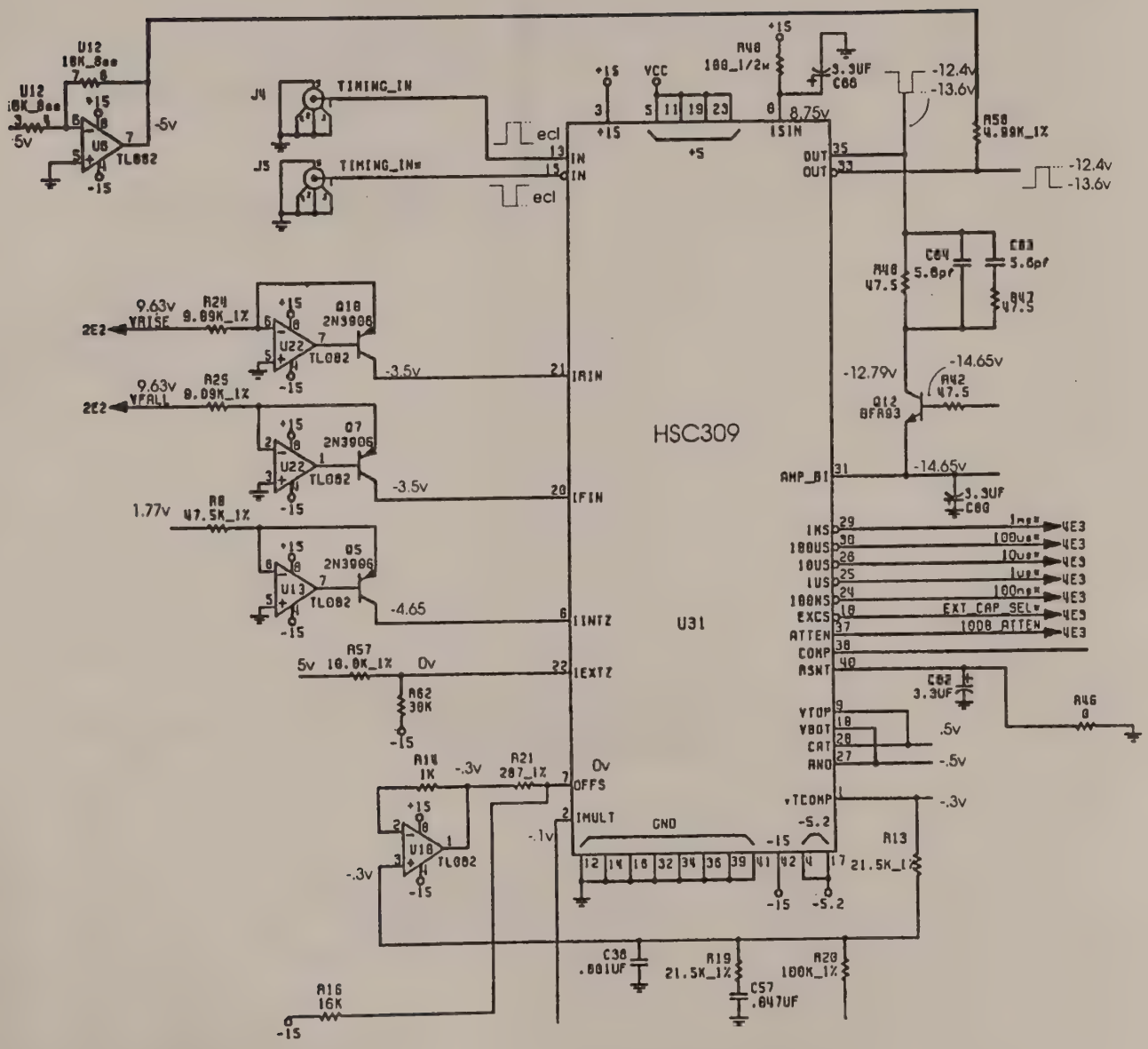
   Once the file is loaded, DO NOT TOUCH ANY front panel controls. The control file has set all of the DAC's to a known state. If the Mainframe detects a change in settings from the front panel, it will reprogram the values loaded into the DAC's based on the power-up calibration.

   Check the DC voltages around the two hybrids (HSC309 & HVV304) and trace schematics (see F6.2.2 A&B), to show the various voltages around the hybrids that were set by the download file.



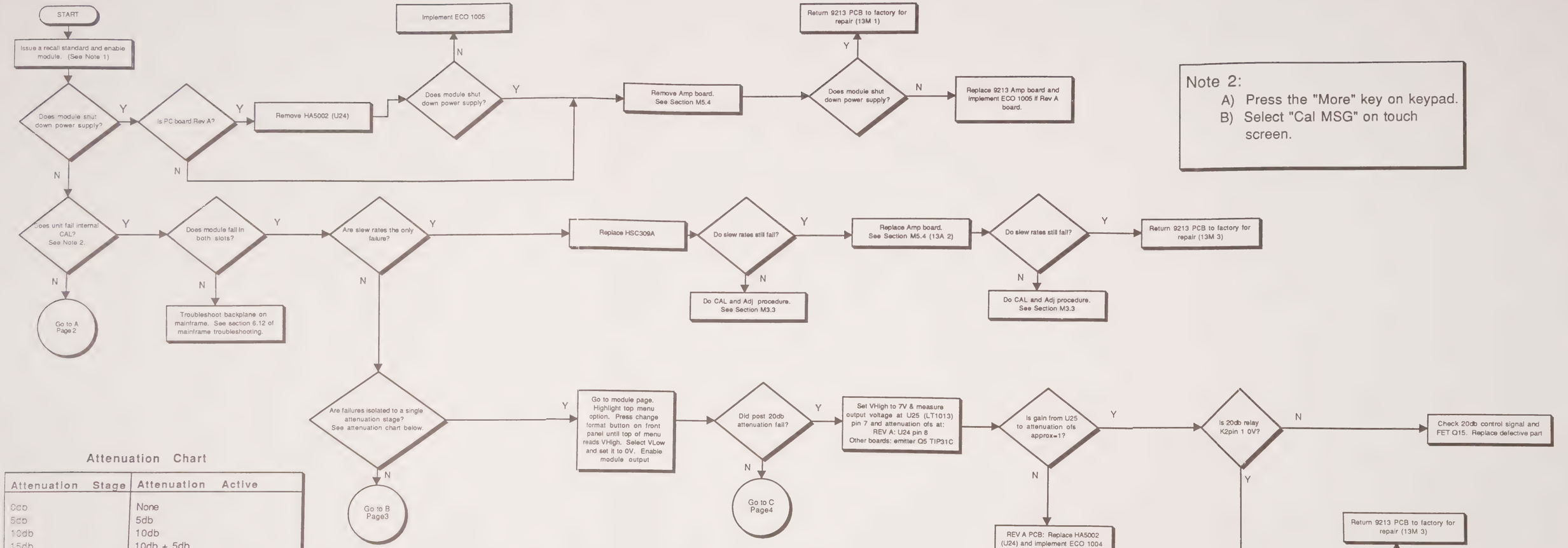
Thermal comp. time constants

F6.2.2A HVV304 Output Amplifier



F6.2.2B HSC309 Slope Generator

M6.4 9213 MODULE



Note 2:

A) Press the "More" key on keypad.
B) Select "Cal MSG" on touch screen.

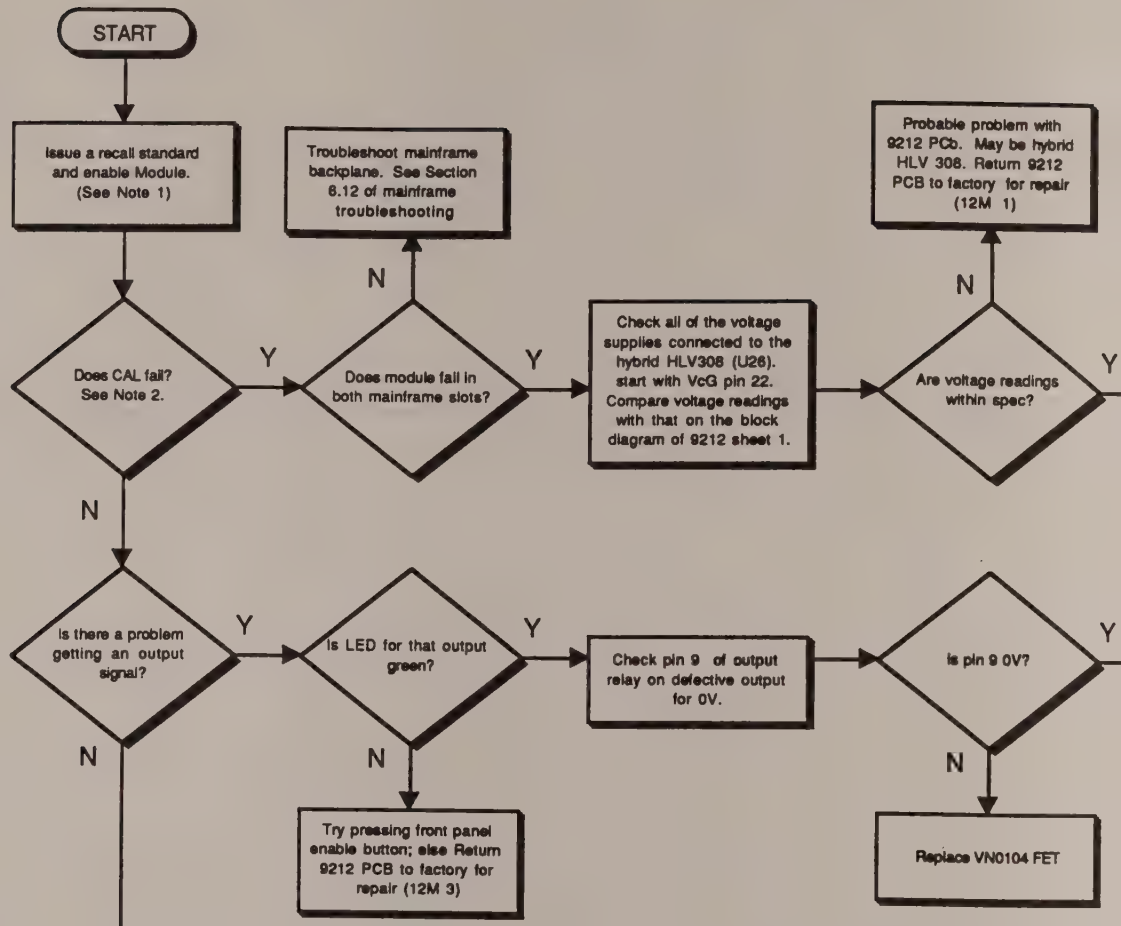
Attenuation Chart

Attenuation Stage	Attenuation Active
0db	None
5db	5db
10db	10db
15db	10db + 5db
20db	pre-20db
25db	pre-20db+5db
30db	pos-20db+10db
35db	pos-20db+10db+5db
40db	pos-20db+pre20db
45db	pos-20db+pre-20db+5db
50db	pos-20db+pre20db+10db
55db	pos-20db+pre20db+10db+5db

Note 1:

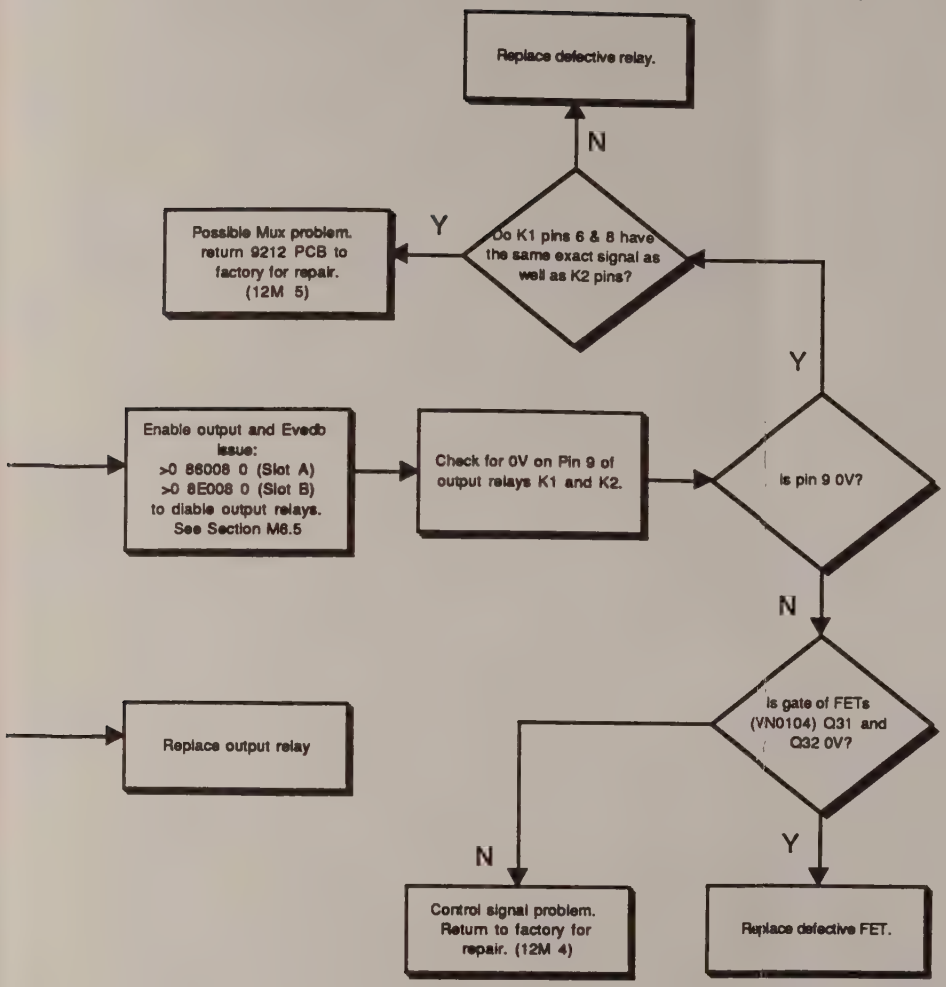
A) Press the "More" key on keypad.
B) Press the "Recall Setup" key on keypad.
C) Select "Standard" on the touch screen.
D) Press "Disable" key on Module keypad.

M6.3
9212 & 9214
MODULE



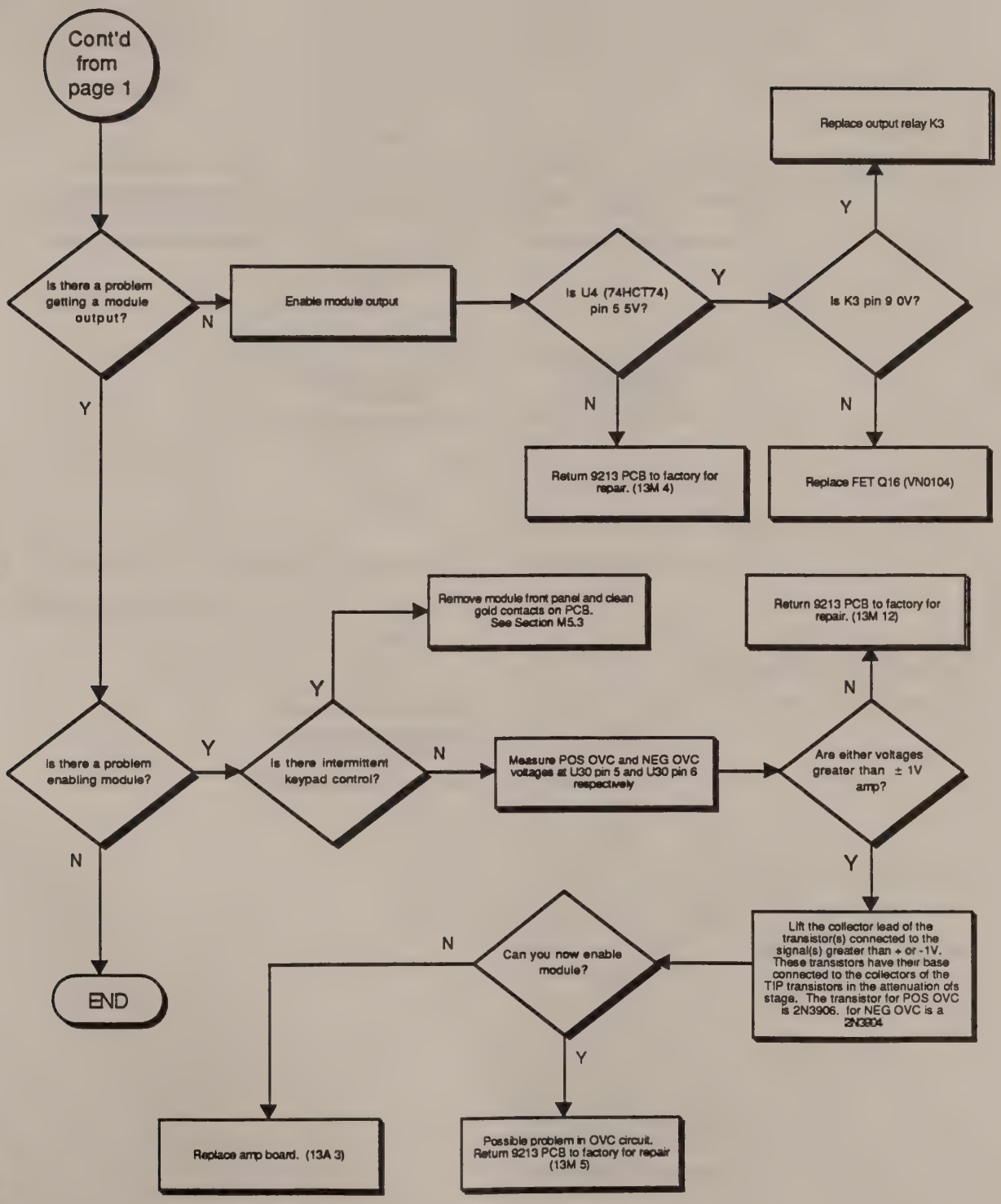
Note 1:

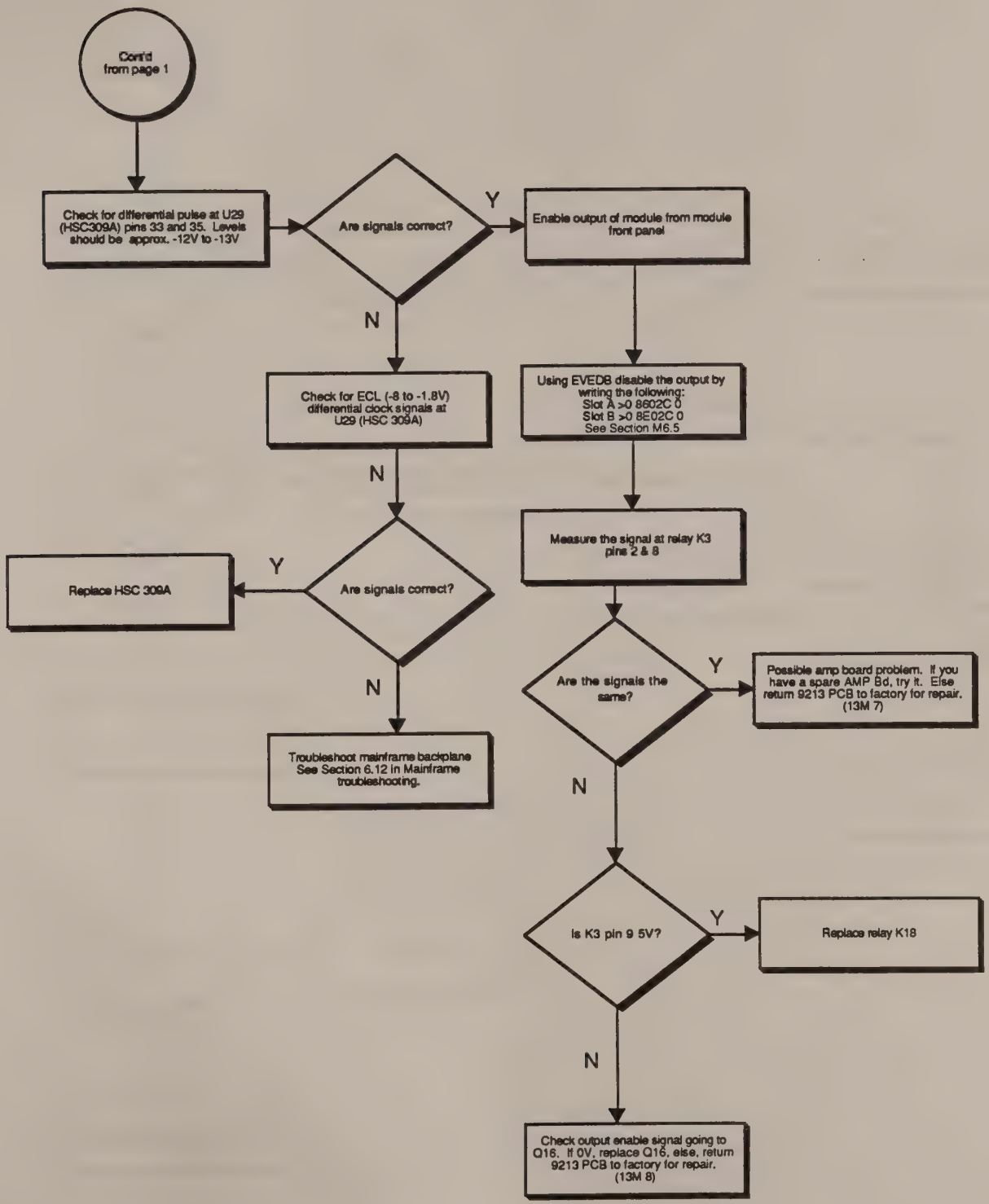
A) Press the "More" key on keypad.
B) Press the "Recall Setup" key on keypad.
C) Select "Standard" on the touch screen.
D) Press "Disable" key on Module keypad.

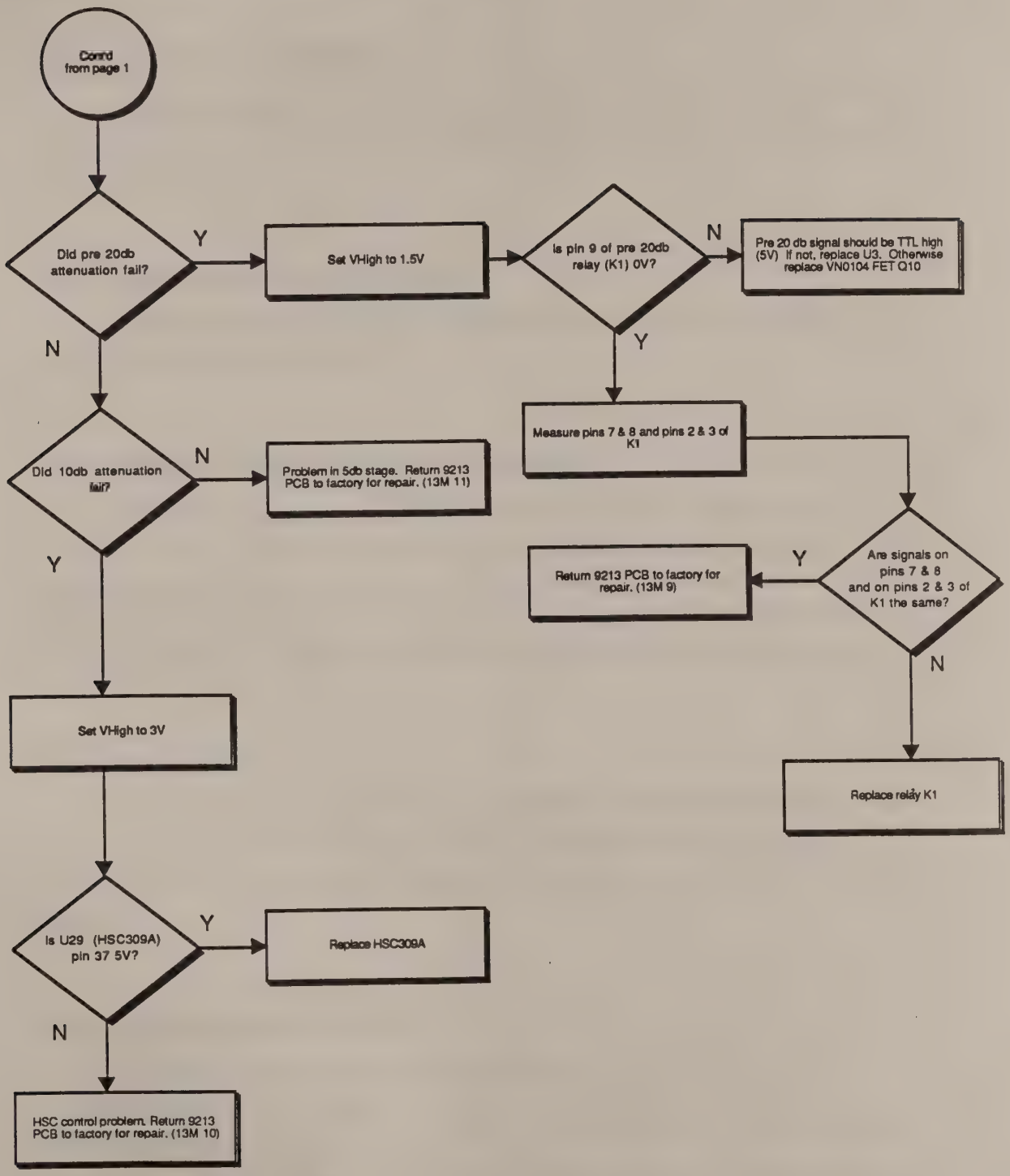


Note 2:

A) Press the "More" key on keypad.
B) Select "Cal MSG" on touch screen.


Cont'd from page 1
Is there a problem getting a module output?
N
Enable module output
Is U4 (74HCT74) pin 5 5V?
Y
Is K3 pin 9 0V?
Y
Replace output relay K3
N
Return 9213 PCB to factory for repair. (13M 4)
N
Replace FET Q16 (VN0104)
Y
Is there a problem enabling module?
Y
Is there intermittent keypad control?
Y
Remove module front panel and clean gold contacts on PCB. See Section M5.3
N
Measure POS OVC and NEG OVC voltages at U30 pin 5 and U30 pin 6 respectively
Are either voltages greater than ± 1V amp?
N
Return 9213 PCB to factory for repair. (13M 12)
Y
Lift the collector lead of the transistor(s) connected to the signal(s) greater than + or -1V. These transistors have their base connected to the collectors of the TIP transistors in the attenuation ofs stage. The transistor for POS OVC is 2N3906. for NEG OVC is a 2N3904
N
Can you now enable module?
Y
N
END
Replace amp board. (13A 3)
Possible problem in OVC circuit. Return 9213 PCB to factory for repair (13M 5)


Cont'd from page 1
Check for differential pulse at U29 (HSC309A) pins 33 and 35. Levels should be approx. -12V to -13V
Are signals correct?
Y
Enable output of module from module front panel
N
Check for ECL (-8 to -1.8V) differential clock signals at U29 (HSC 309A)
Using EVEDB disable the output by writing the following:
Slot A >0 8602C 0
Slot B >0 8E02C 0
See Section M6.5
N
Measure the signal at relay K3 pins 2 & 8
Are signals correct?
Y
Replace HSC 309A
N
Troubleshoot mainframe backplane See Section 6.12 in Mainframe troubleshooting.
Are the signals the same?
Y
Possible amp board problem. If you have a spare AMP Bd, try it. Else return 9213 PCB to factory for repair. (13M 7)
N
Is K3 pin 9 5V?
Y
Replace relay K18
N
Check output enable signal going to Q16. If 0V, replace Q16, else, return 9213 PCB to factory for repair. (13M 8)


Contd from page 1
Did pre 20db attenuation fail?
Y
Set VHigh to 1.5V
Is pin 9 of pre 20db relay (K1) 0V?
N
Pre 20 db signal should be TTL high (5V) If not, replace U3. Otherwise replace VN0104 FET Q10
Y
N
Measure pins 7 & 8 and pins 2 & 3 of K1
Did 10db attenuation fail?
N
Problem in 5db stage. Return 9213 PCB to factory for repair. (13M 11)
Y
Are signals on pins 7 & 8 and on pins 2 & 3 of K1 the same?
Y
Return 9213 PCB to factory for repair. (13M 9)
N
Replace relay K1
Set VHigh to 3V
Is U29 (HSC309A) pin 37 5V?
Y
Replace HSC309A
N
HSC control problem. Return 9213 PCB to factory for repair. (13M 10)

6.5 9210 COMMUNICATION SOFTWARE (EVEDB)

6.5.1 Utility Programs Installation

The utility programs are contained on a High Density diskette attached to the back flap of this mannual. The utility programs can be run directly from the floppy or copied to a hard drive.

6.5.2 Communication Software (EVEDB.EXE)

This section contains information about EVEDB.EXE, which is distributed free with the 9210 Service Manual.

6.5.3 Disclaimer of Warranty and Implied Warranty

EVEDB.EXE and accompanying files are provided "as is" without warranty of any kind. LeCroy Corporation disclaims all warranties, either express or implied, including but not limited to implied warranties of fitness for a particular purpose, with respect to EVEDB.EXE and accompanying files, and the diskette they are delivered on. The entire risk as to the results and performance of EVEDB.EXE is assumed by you.

6.5.4 Requirements

EVEDB.EXE runs on IBM-PCs and compatibles. EVEDB.EXE requires a National Instruments GPIB card at address 0, and National Instrument's handler, GPIB.COM, loaded into memory. EVEDB.EXE has been used with PCII and AT-GPIB cards.

6.5.5 Why We Distributed EVEDB.EXE

EVEDB.EXE permits use of Gpib to communicate with an IEEE-488.2 compatible instrument in a convenient, conversational manner. In addition, there is special support for reading error messages from a LeCroy 9210 pulse generator, which provides more detailed messages in addition to the IEEE-488.2 standard error reporting mechanism.

6.5.6 Overview of EVEDB Operation

At EVEDB's "Command > " prompt, any entry of more than one consecutive non-blank character is sent directly to the 9210. If there is a response or if an error occurs the appropriate action is automatically taken, that is, the response is read back or the standard Event Status Register (and specific error message, from the LeCroy 9210) is read back.

At EVEDB's "Command > " prompt, any entry of only one non-blank character is considered a command for EVEDB.EXE; it is not sent to the 9210. Commands you might use are:

'q' :	Quit.	Exit EVEDB.
'f':	File.	"f filename" sends the text file "filename" to the 9210. Each line is sent as a seperate message.
'0' :	Re-initialize.	If the 9210 has been turned off and then turned back on while EVEDB was running, '0' will restablish communication (by re-enabling specific causes of SRQ in the device). It also re-displays EVEDB's command menu, shown below. This command may be used at any time; it is only necessary if the device has been turned off and on.
't' :	Transcript.	Toggles transcript on/off. When transcript is enabled, all GPIB transactions are copied to file EVEDB.LOG. When transcript is enabled for the first time after executing EVEDB, the file EVEDB.LOG is created empty. While EVEDB is running, transcript may be enabled and disabled; information is appended to EVEDB.LOG.

EVEDB.EXE also has capabilities for lower level debugging, such as reading and writing to memory within the 9210, and using symbol tables for referring to memory locations by name. We do not expect users to make much use of these features. Please use EVEDB's help message (by executing "evedb -h") for further information on these features.

6.5.7 Running EVEDB.EXE

Example calls:

EVEDB

Device is assumed to be at address 1.

EVEDB shows:

"For help message, restart this program 'C:\EVEDB.EXE -h' 0:menu/reinit
Q:Quit I:read O:write M:inspect N: size for M,I,O F:send file S:symbol value
A: Address symbol name
Command > "

EVEDB -h

Prints a detailed help message, followed by the menu and "Command>" prompt shown above. You may capture the help message to a disk file by typing "EVEDB -h > file" followed by <Enter>, then 'q' followed by <Enter> to exit EVEDB.

EVEDB -a4

Device is assumed to be at address 4.

EVEDB -symbol.map -a4

Loads a symbol table "symbol.map", talk to device at address 4.

Press "q" to exit EVEDB.

6.5.8 General rules:

1. Any command of more than one character is assumed to be a command for the 9210. All rules to follow apply only to the single-character commands listed for EVEDB, listed in the menu shown above.

2. If a symbol table (.MAP file) has been loaded, symbol names may be used where an address is required. Addresses may only be HEX values or symbol names. Please see the help message (use EVEDB -h) for more information about the use of symbols tables.

3. You may add dummy symbols to the .MAP file, for your convenience (see section 6.5.1). The .MAP file is pure ASCII, and contains 4 fields per line. Only the symbol name and value, the 1st and 3rd fields, are used by EVEDB. Symbol names MUST NOT begin with a valid hex digit.

   Note ***The first two lines of the symbol table MUST be exactly the same as in the supplied example, SYMBOL.MAP.***

4. Data is assumed to be hex, unless it is followed by a '.', in which case it is interpreted as decimal. EVEDB shows data in hex and decimal using this format.

   Note ***All values are unsigned.***

5. Error messages are preceded by '***'. Error messages of the form "*** Error: < number >,<string in all capital letters>" show an error message from the 9210 in response to a command. An example would be "*** Error: 102, SYNTAX ERROR."

6.5.9 Using EVEDB

Here is an example of what you should see when talking to a 9210 using EVEDB with Gpib commands:

Command > ***IDN?**	*(Executes a 9210 command)*
LECROY, 9210, 0, 910418	*(answer or error message, if any)*
Command > ***CAL?**	*(Query which takes a long time)*
16	*(Here is the answer to *CAL?)*
Command > **t**	*(Transcript file on/off.)*
Command > **m _CHAR_RAM_BASE**	*(Memory inspect/modify using symbol)*
_CHAR_RAM_BASE C7800	*(Symbol's value (ie, address) shown)*
C7800 00 0.	*(Hex and decimal. CR to leave this value alone.)*
C7801 00 0. 41	*(Specify a new value for this address)*
C7801 41 65.	*(Verify)*
C7802 00 0. q	*(Invalid hex data to exit memory modify)*
Command > q	*(Exit EVEDB.EXE)*

Please refer to the Model 9210 Operator's Manual for documentation of Gpib commands.

To see an example of 9210 commands which can set the 9210 to its current state, please use the IEEE-488.2 common query "*LRN?".

The example using the symbol _CHAR_RAM_BASE assumes that the example symbol table, SYMBOL.MAP, was loaded by EVEDB. Otherwise, "m C7800" could have been used.

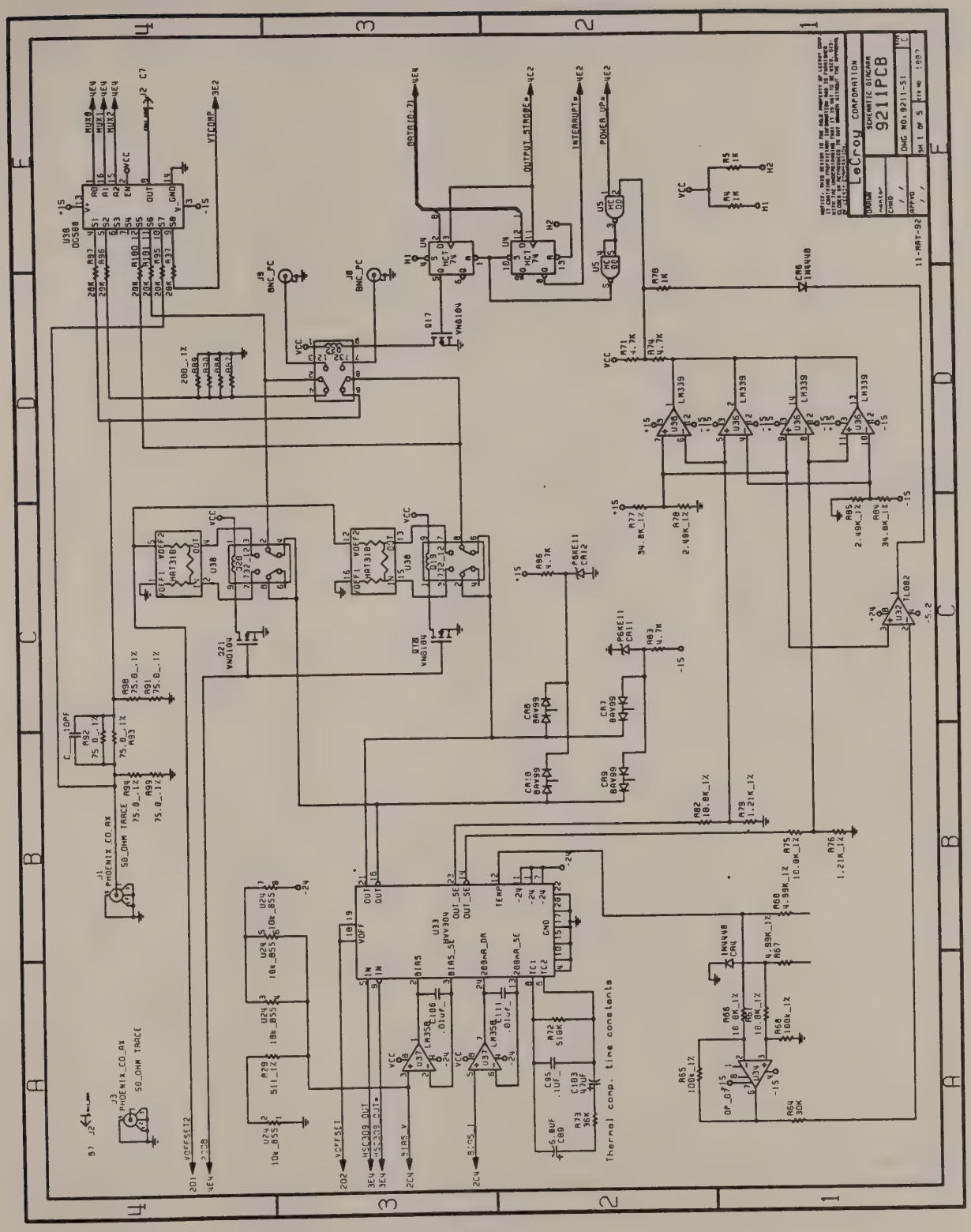
6.6 9211 Control File (9211.CTL)

This file contains commands that directly control the hardware of the 9211 module. It is used to overwrite the data, from the module calibration routine, written to the control DAC's of the 9211 module. This allows the service personnel to deal with known control voltages instead of calculated control voltages.

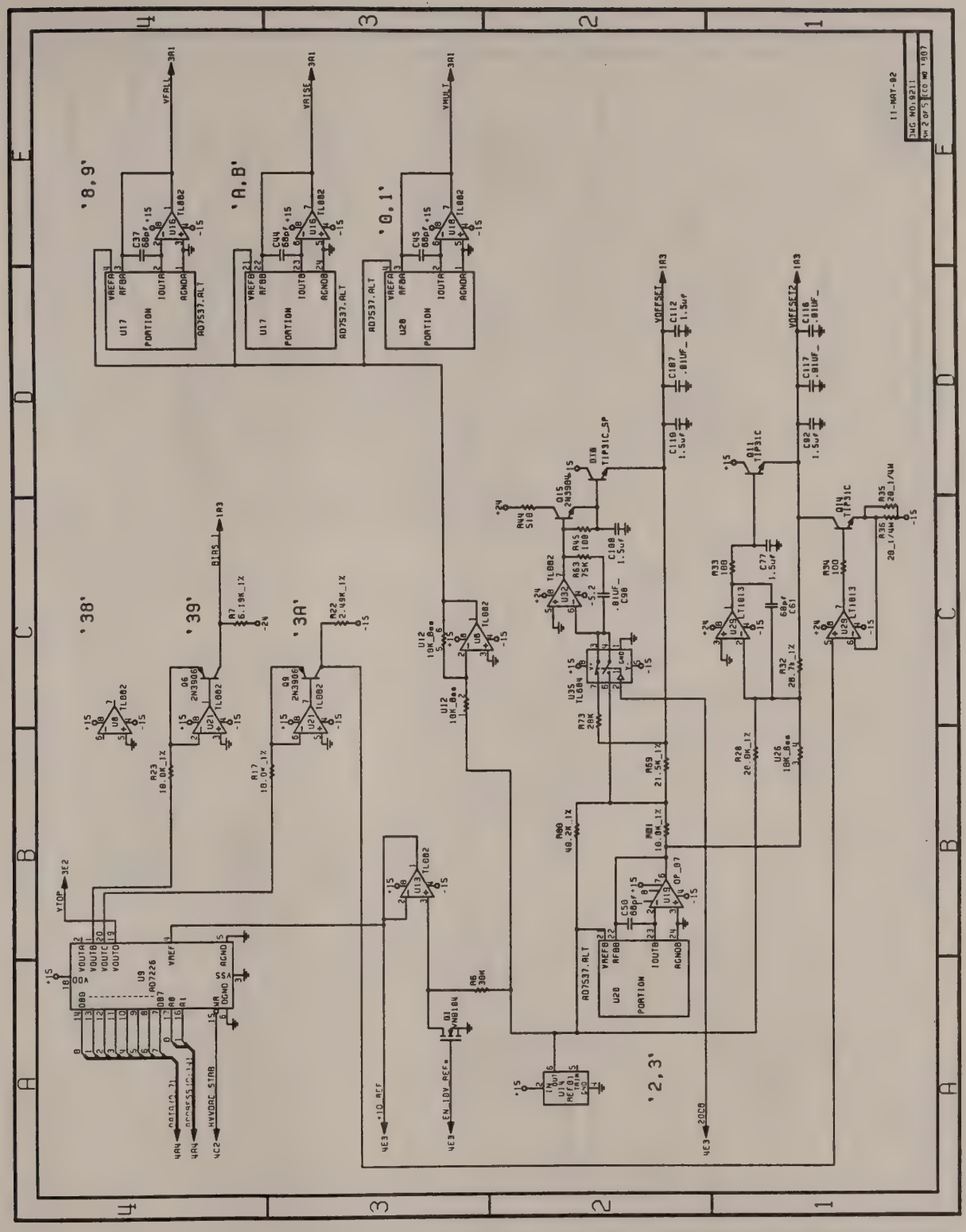
6.7 Example of a Symbol Table (Symbol.Map)

The following table is a duplicate of the file SYMBOL.MAP located on the Utilities Program Disk.

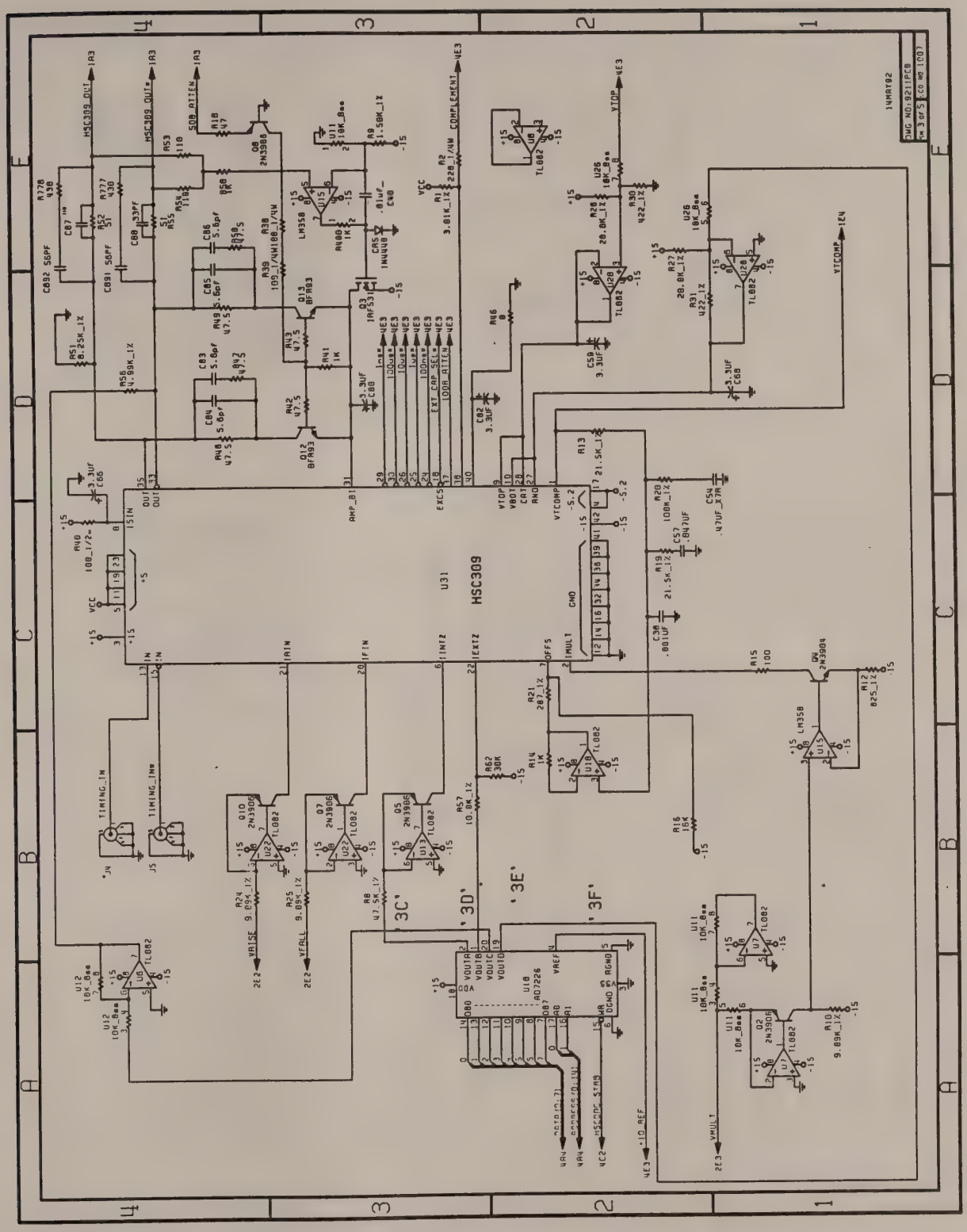
NAME	CLASS	VALUE	REGION
_BASE_PROM	reloc	00000H	code
_BASE_RAM	reloc	40000H	ram
_BASE_BRAM	reloc	7C000H	battery_ram
_PLUG_A_BASE	reloc	80000H	none
_PLUG_B_BASE	reloc	88000H	none
_MEASURE_BASE	reloc	90000H	none
_LED_BASE	reloc	91000H	none
_FRONT_PANEL_CONTROL	reloc	92000H	none
_BASE_9914	reloc	94000H	none
_BASE_68901	reloc	95000H	none
_HW_STATUS_LATCH	reloc	96000H	none
_TIMING_A_BASE	reloc	98000H	none
_TIMING_B_BASE	reloc	9A000H	none
_PERIOD_GEN_BASE	reloc	9C000H	none
_FONT_ROM_BASE	reloc	A0000H	none
_VIDEO_RAM_BASE	reloc	C0000H	none
_CHAR_RAM_BASE	reloc	C7800H	none



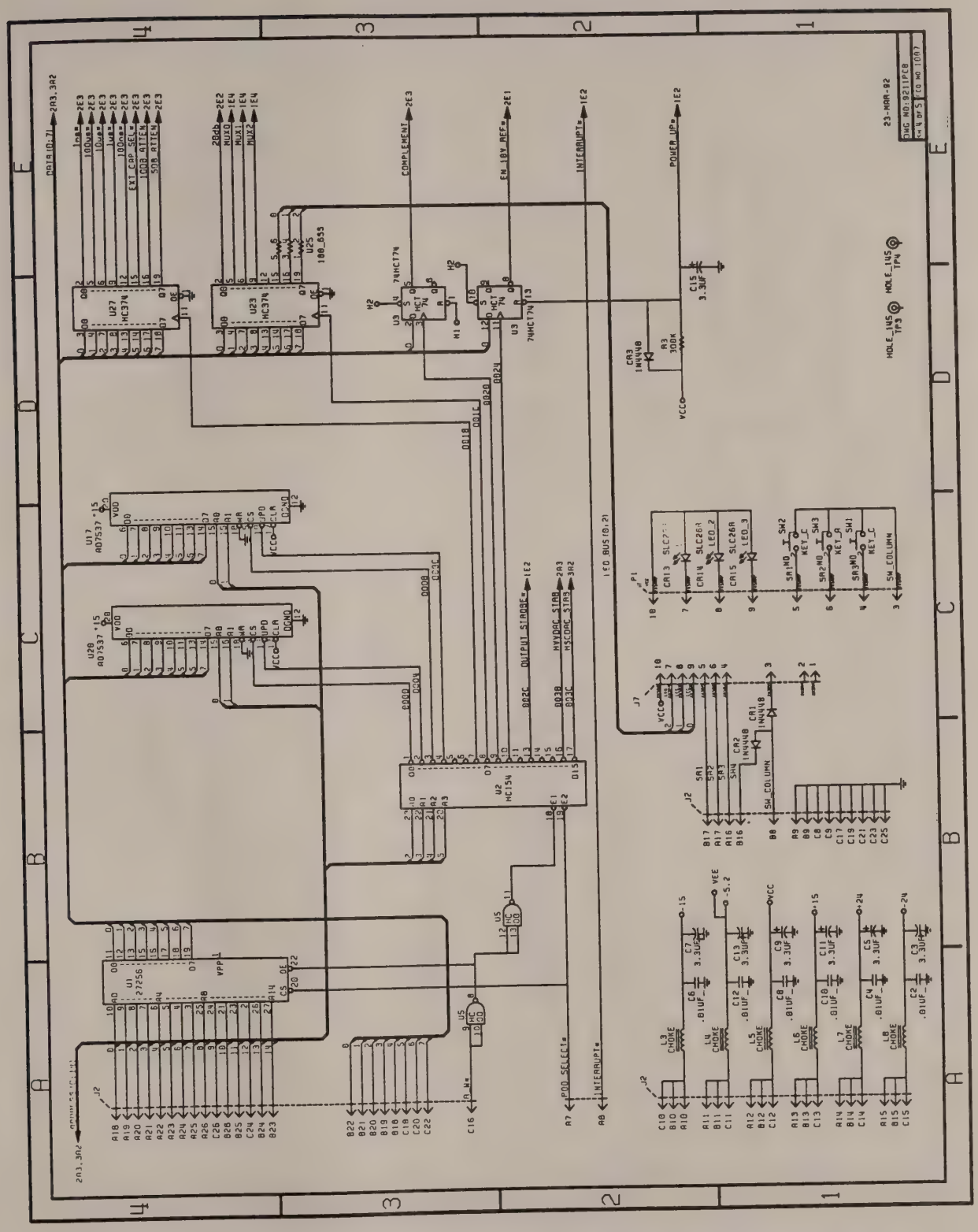
S1 9211 PCB Schematics Rev A-1



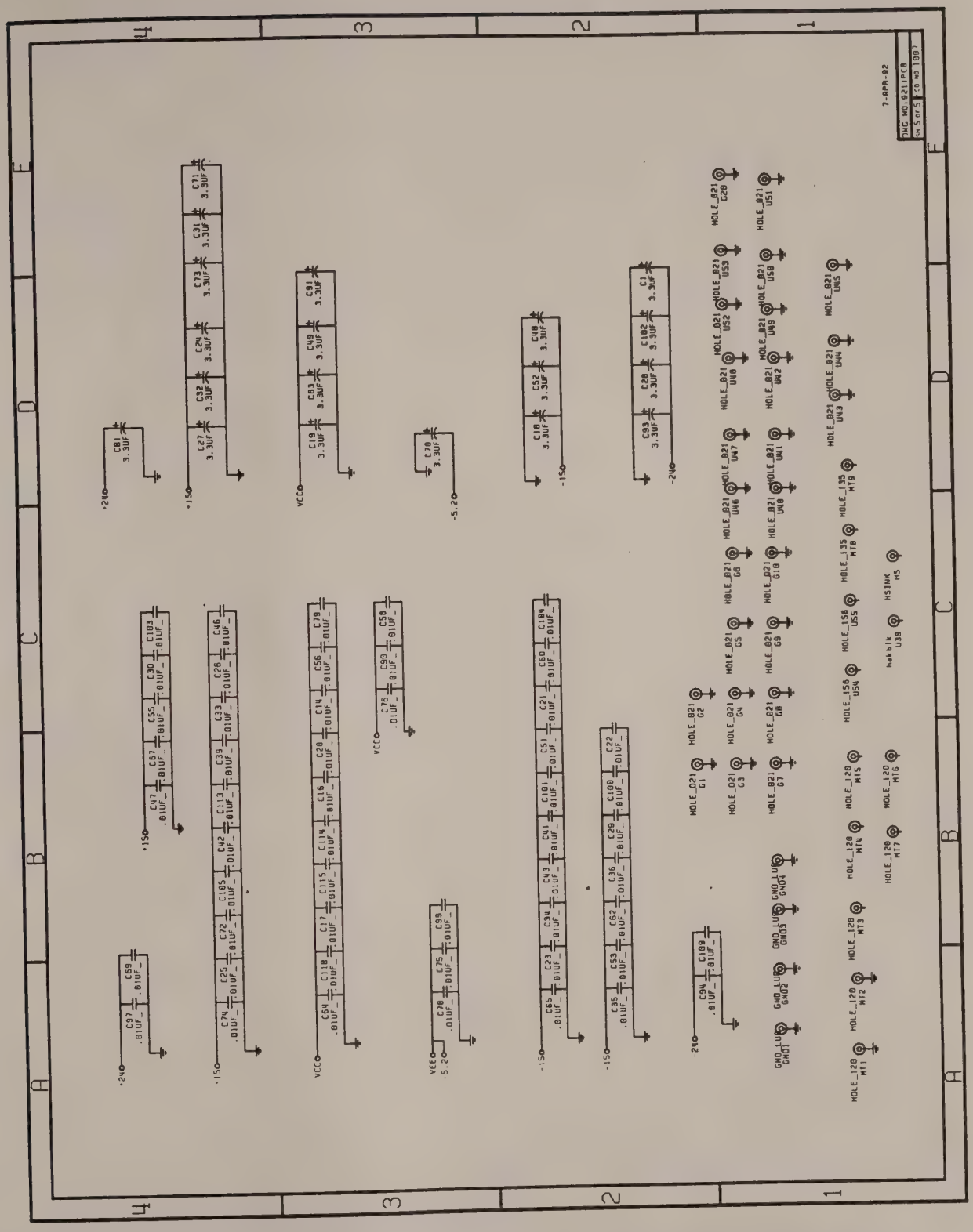
S2 9211 PCB Schematics Rev A-2



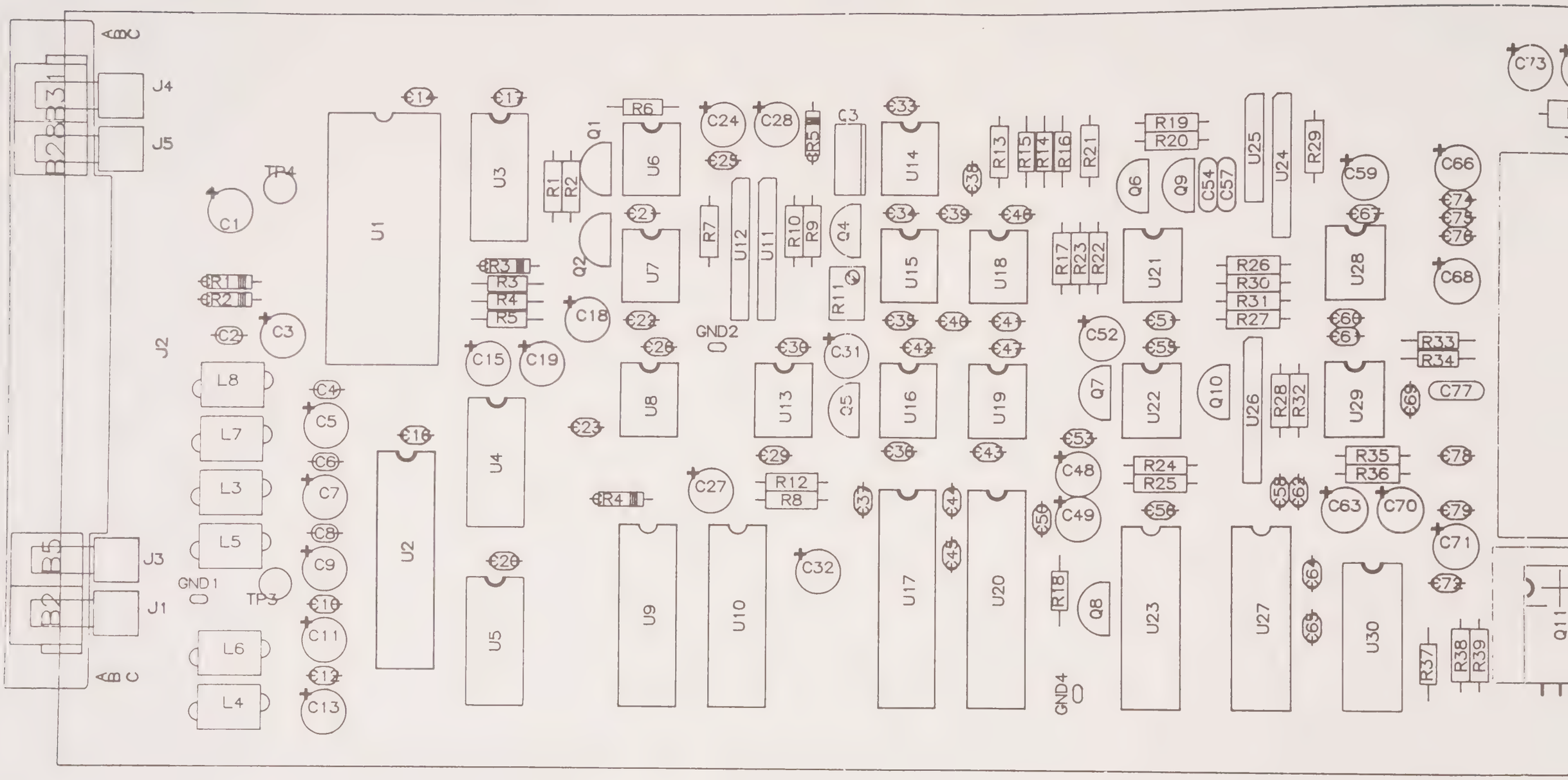
S3 9211 PCB Schematics Rev A-3



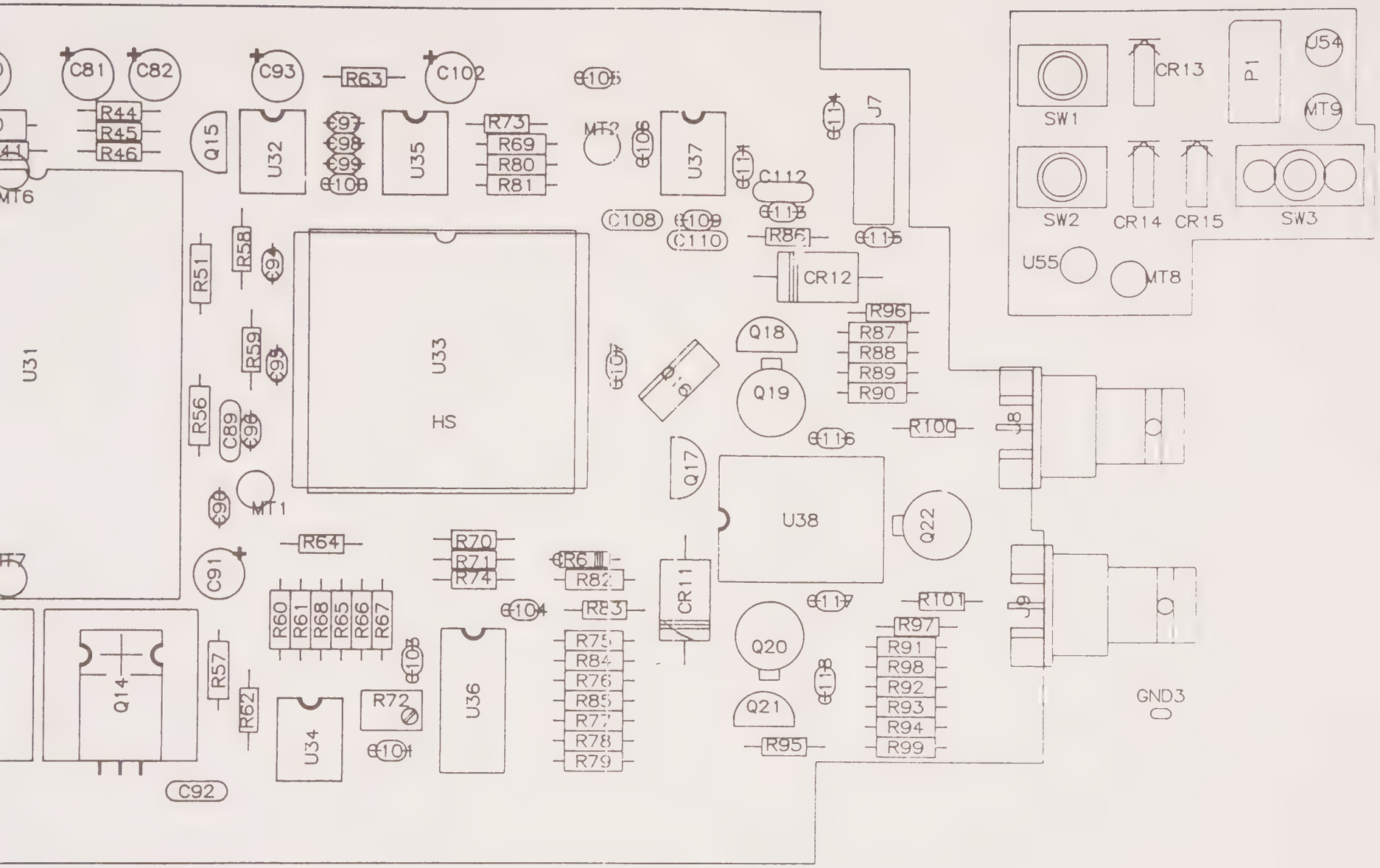
S4 9211 PCB Schematics Rev A-4

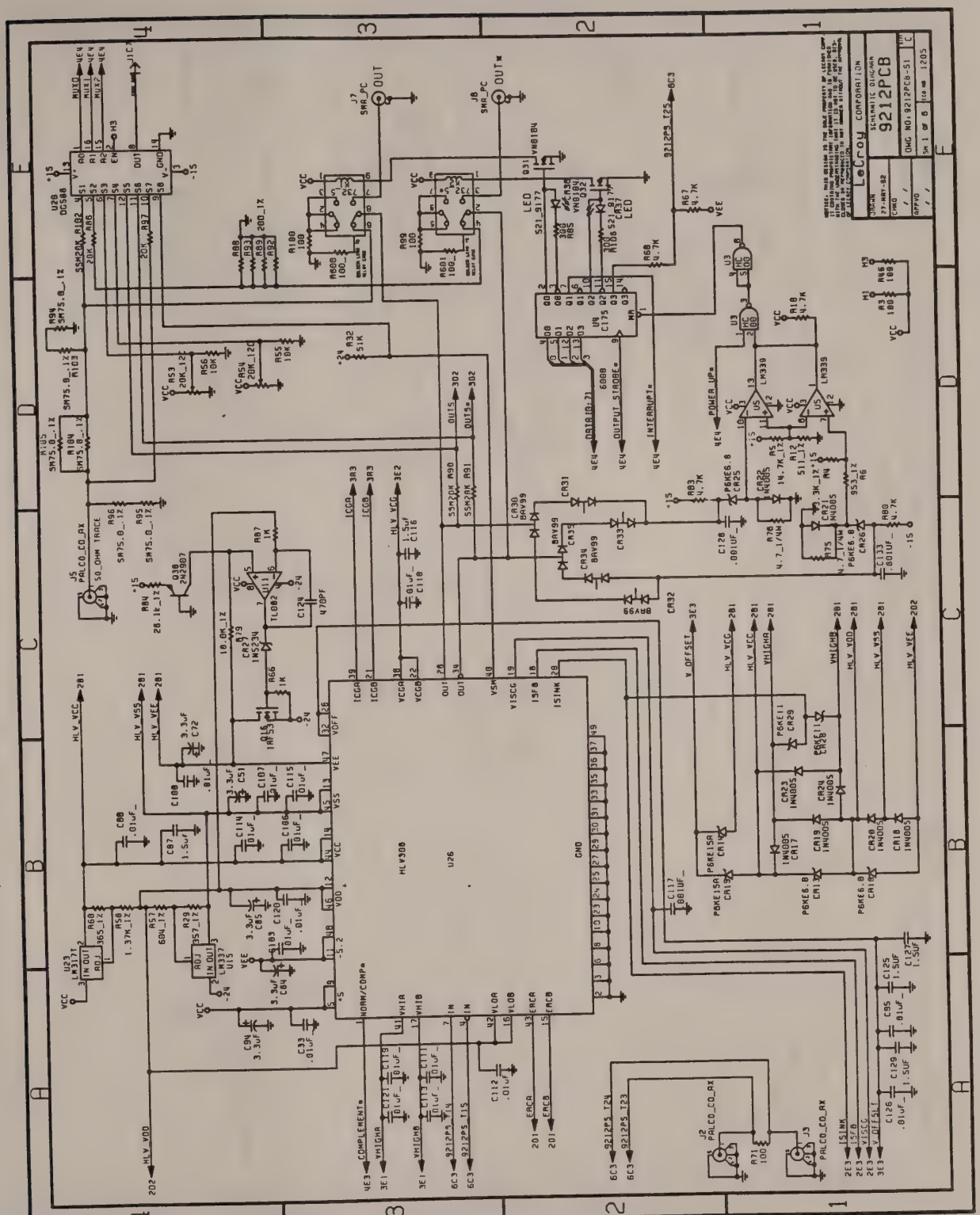


S5 9211 PCBSchematics Rev A-5

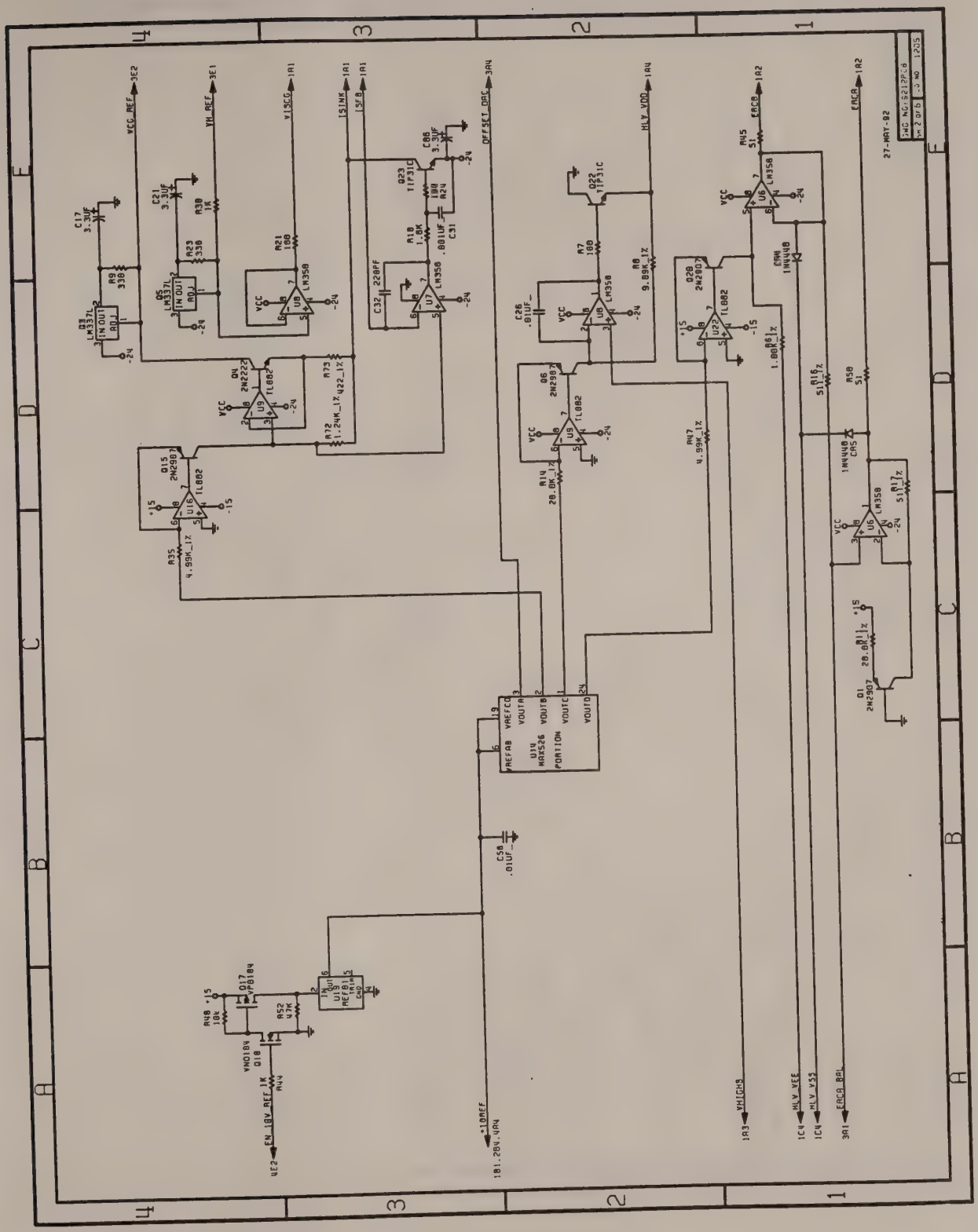

J4
J5
J2
J3
J1
B2
B5
B3
B1
TP4
TP3
GND1
GND2
GND4
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U21
U22
U23
U24
U25
U26
U27
U28
U29
U30
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
C1
C2
C3
C4
C5
C6
C7
C8
C9
C11
C13
C15
C18
C19
C24
C27
C28
C31
C32
C48
C49
C52
C54
C57
C59
C63
C66
C68
C70
C71
C73
C77
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32
R33
R34
R35
R36
R37
R38
R39
L3
L4
L5
L6
L7
L8

9211PCB

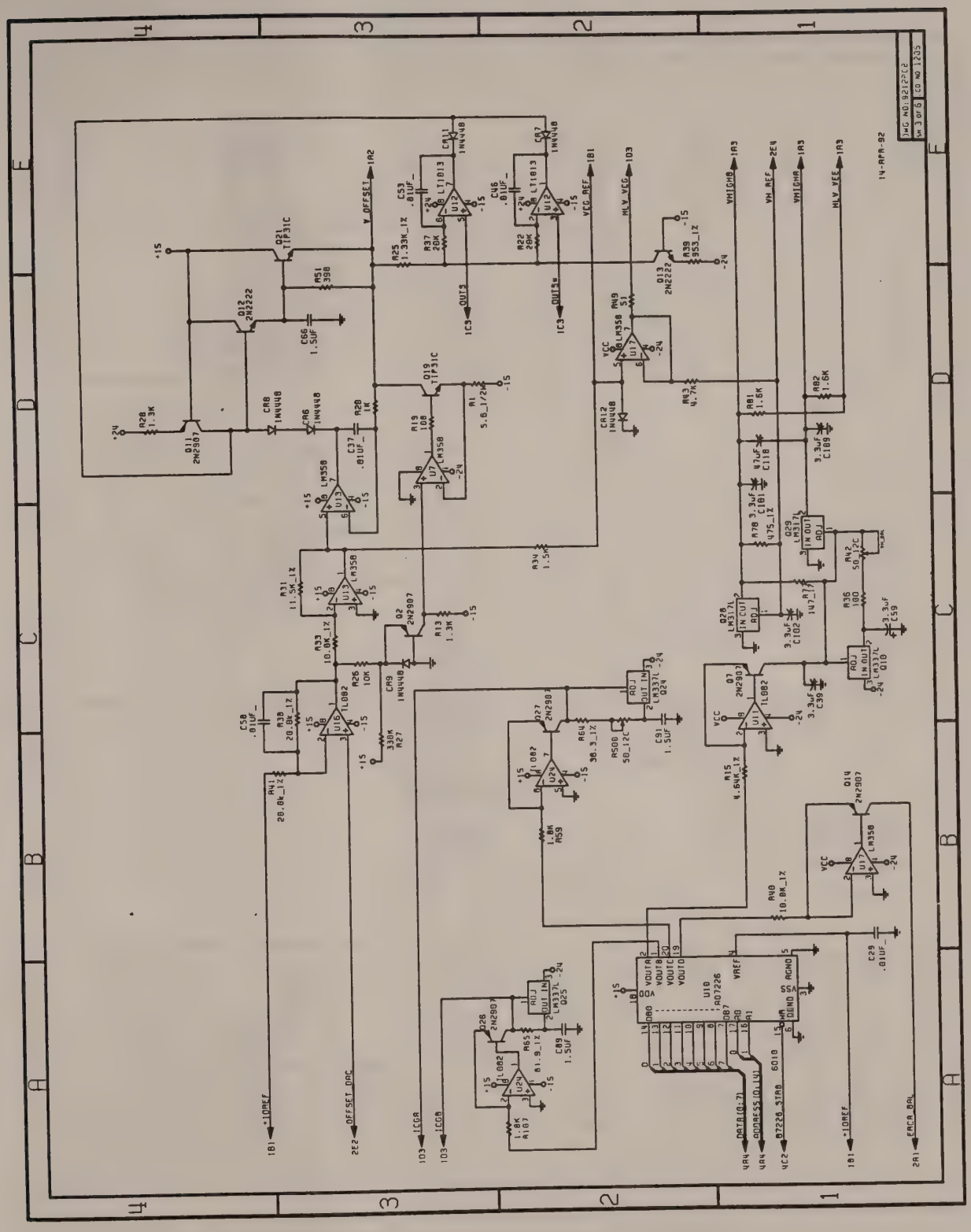

C81
C82
C93
R63
C102
R44
R45
R46
Q15
U32
U35
R73
R69
R80
R81
MT3
U37
C112
J7
C108
C109
C110
R86
CR12
R58
R51
R59
R56
C89
U33
HS
R96
R87
R88
R89
R90
Q18
Q19
R100
J8
Q17
U38
Q22
MT1
R64
R70
R71
R74
R82
R83
CR11
R60
R61
R68
R65
R66
R67
R72
U36
R75
R84
R76
R85
R77
R78
R79
Q20
Q21
R95
R97
R91
R98
R92
R93
R94
R99
R101
J9
GND3
SW1
CR13
P1
U54
MT9
SW2
CR14
CR15
SW3
U55
MT8
U31
Q14
R57
R62
C91
C92



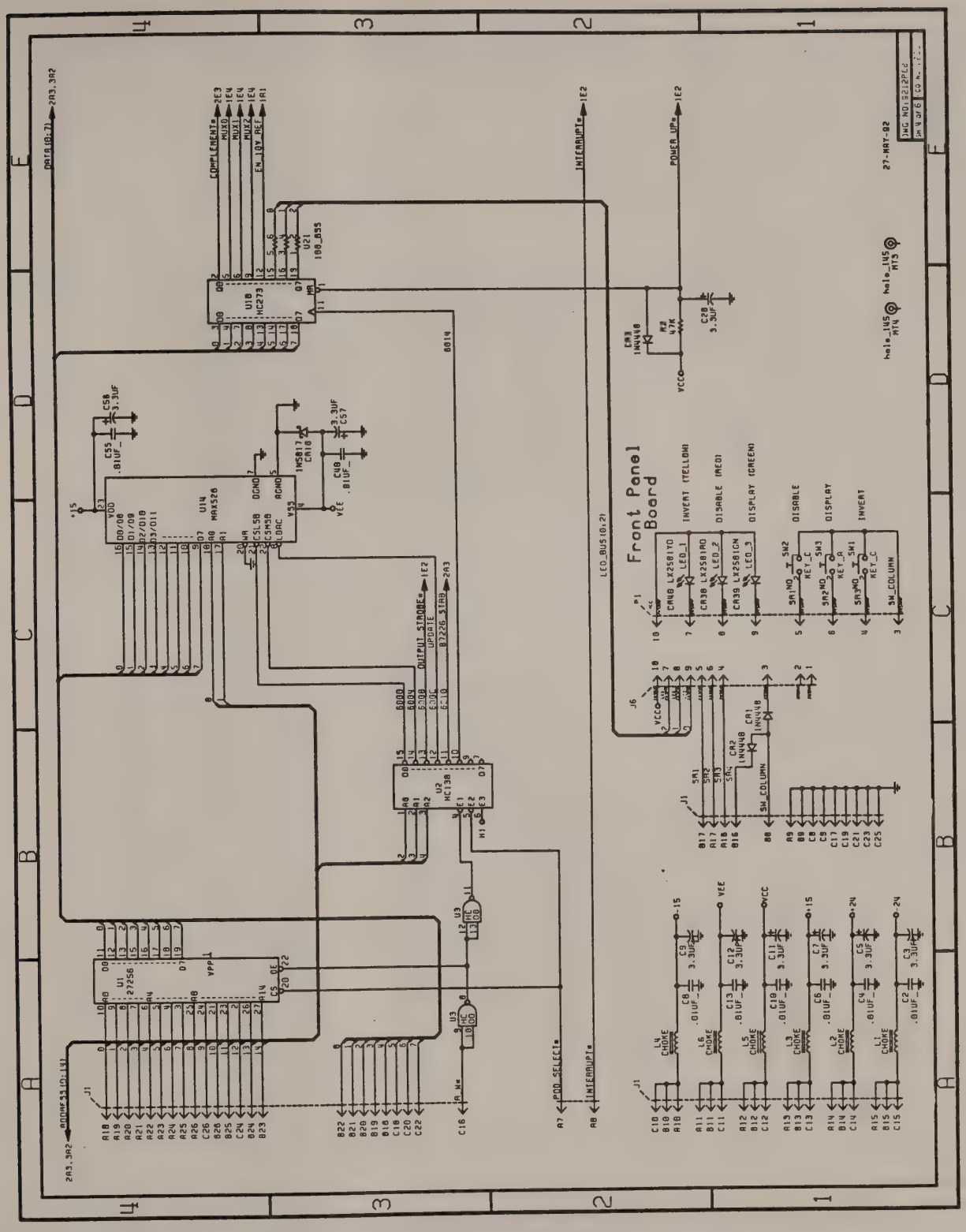
S6 9212 PCB Schematics Rev C-1



S7 9212 PCB Schematics Rev C -2

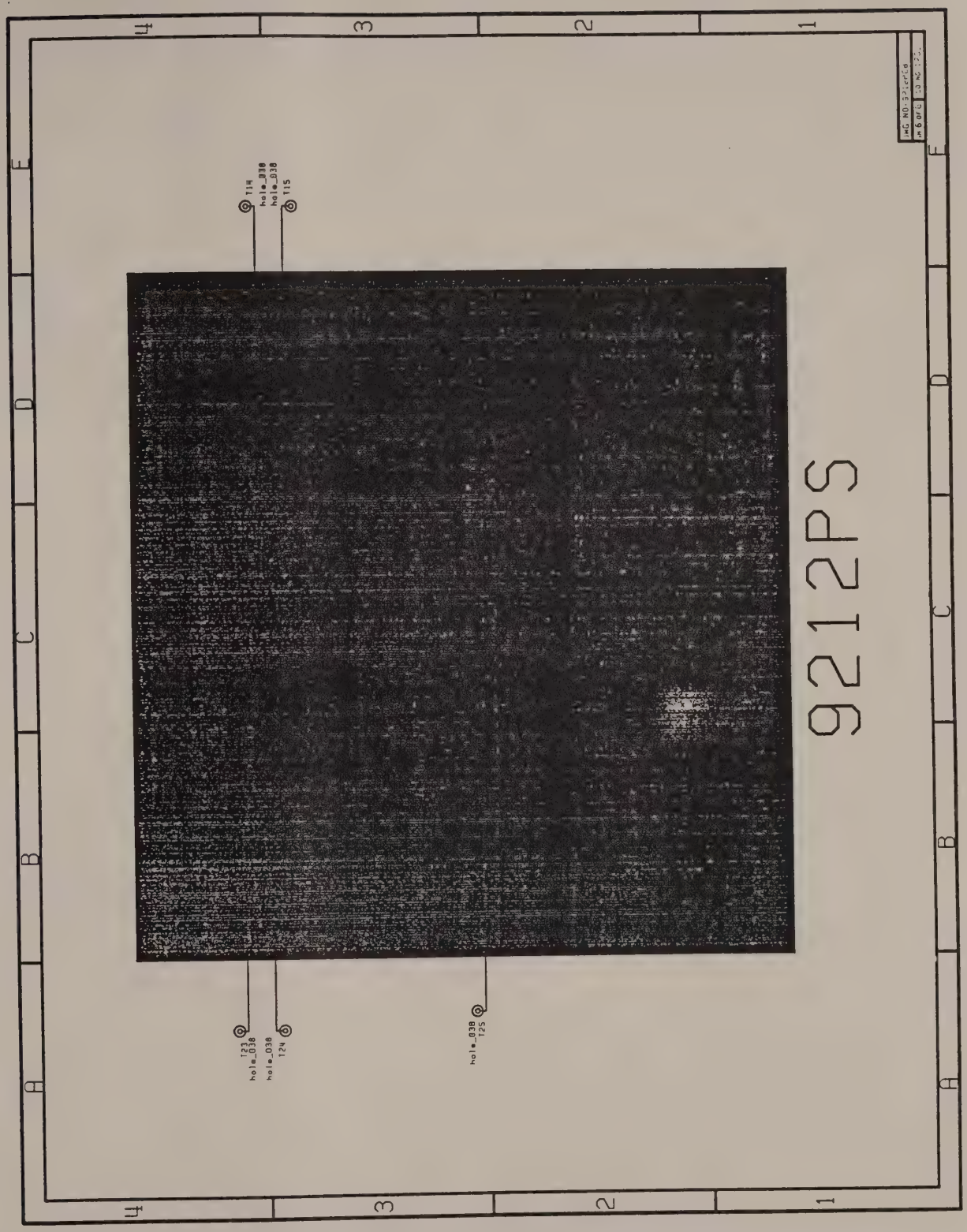


S8 9212 PCB Schematics Rev C-3

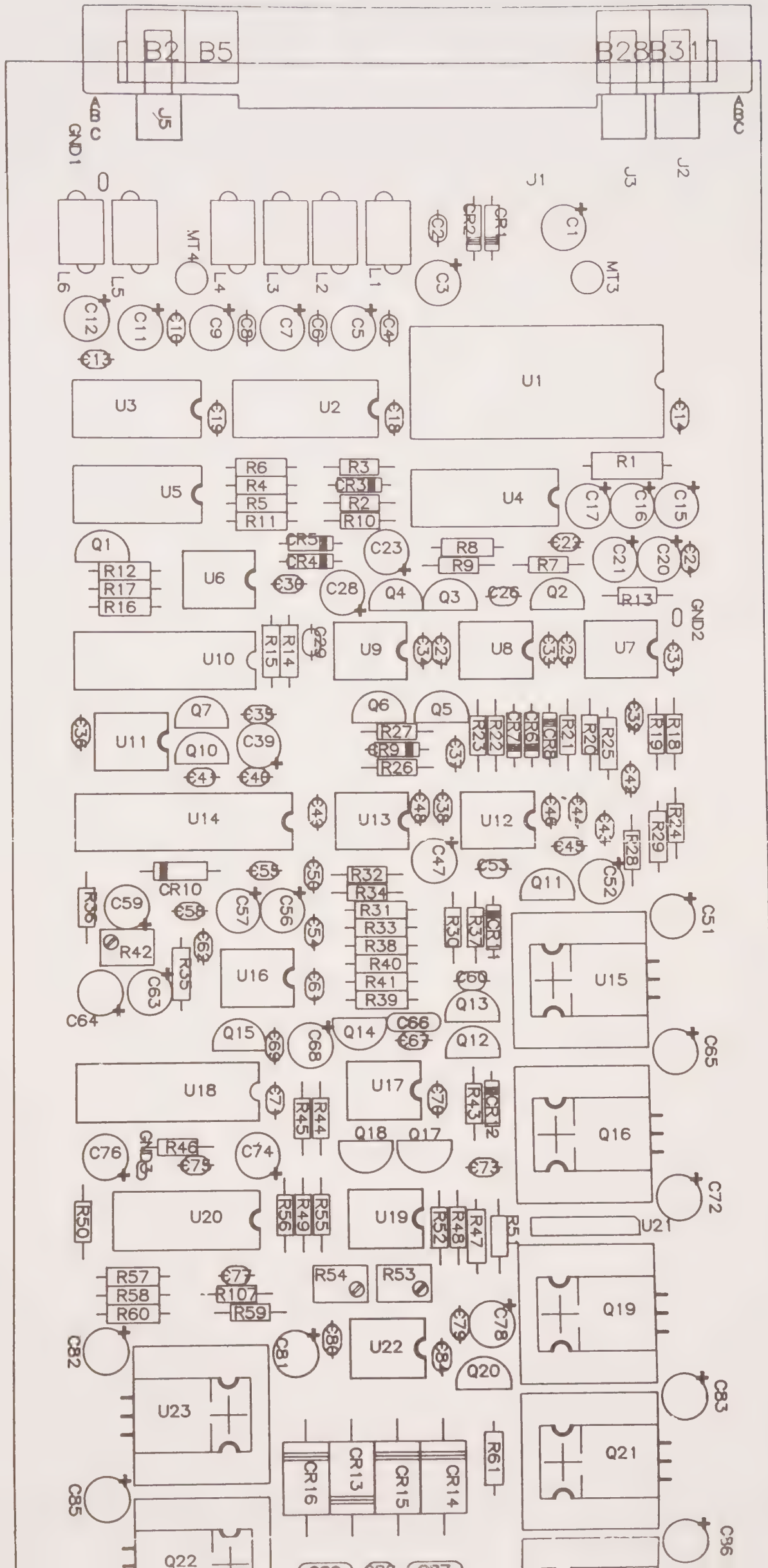


S9 9212 PCB Schematics Rev C-4

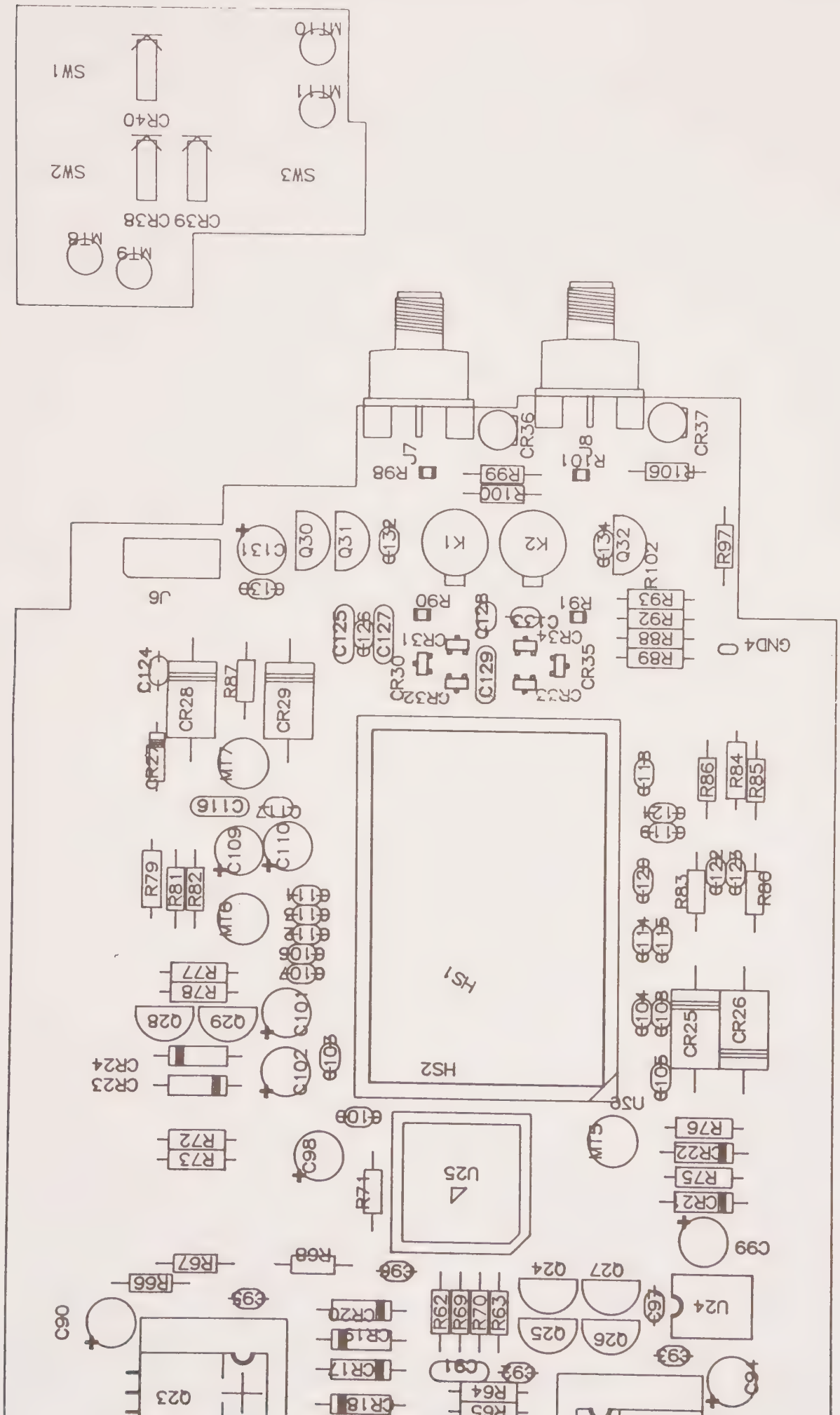
S10 9212 PCB Schematics Rev C-5



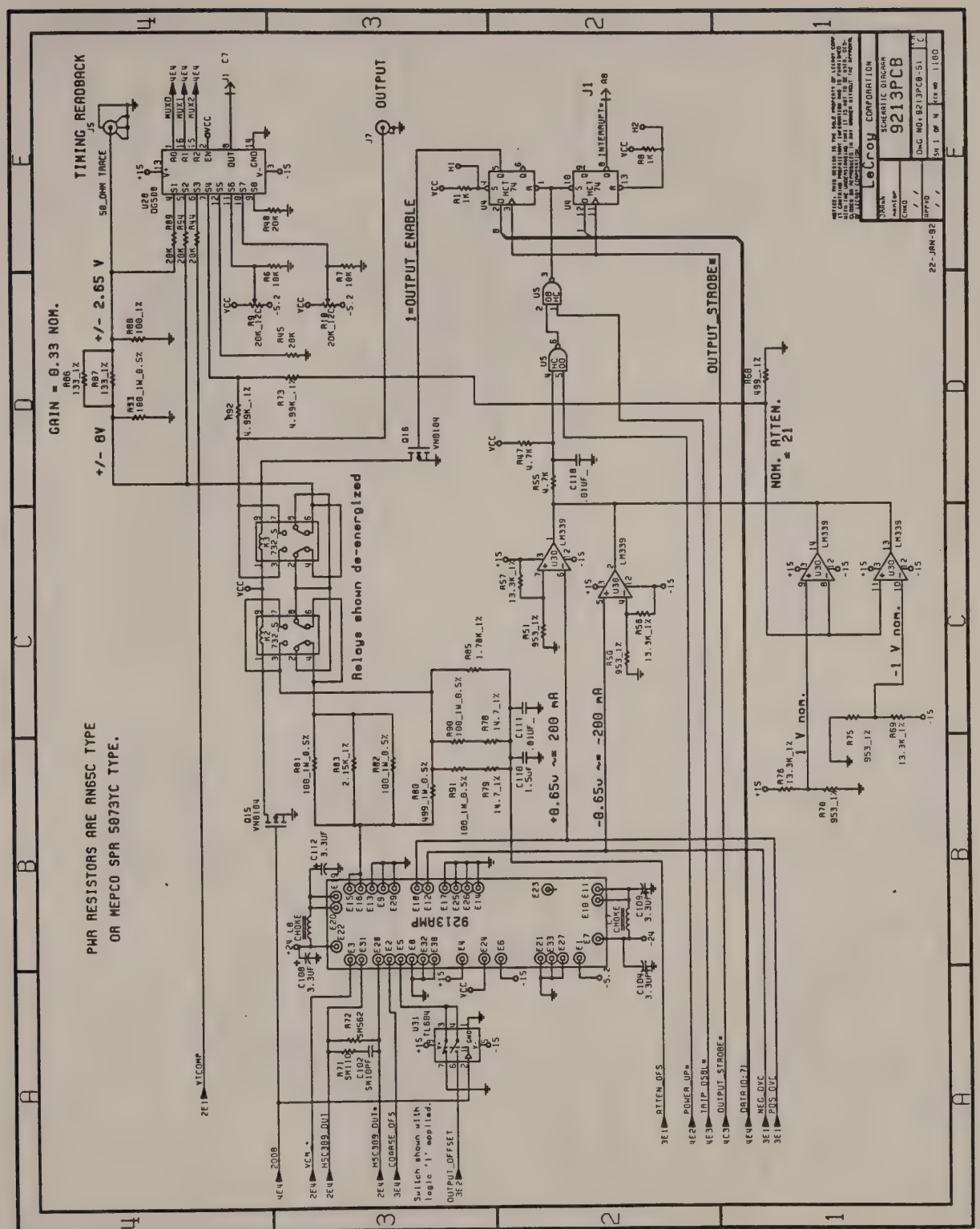
S11 9212 PCB Schematics Rev C-6


B2
B5
B28
B31
J5
J1
J3
J2
GND1
GND2
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U21
U22
U23
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
C1
C2
C3
C4
C5
C6
C7
C8
C9
C11
C12
C15
C16
C17
C20
C21
C23
C28
C39
C47
C51
C52
C56
C57
C59
C63
C64
C65
C66
C68
C72
C74
C76
C78
C81
C82
C83
C85
C86
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32
R33
R34
R35
R36
R37
R38
R39
R40
R41
R42
R43
R44
R45
R46
R47
R48
R49
R50
R52
R53
R54
R55
R56
R57
R58
R59
R60
R61
R107
R14
R15
CR1
CR2
CR3
CR4
CR5
CR6
CR7
CR8
CR10
CR11
CR12
CR13
CR14
CR15
CR16
MT3
MT4
L1
L2
L3
L4
L5
L6

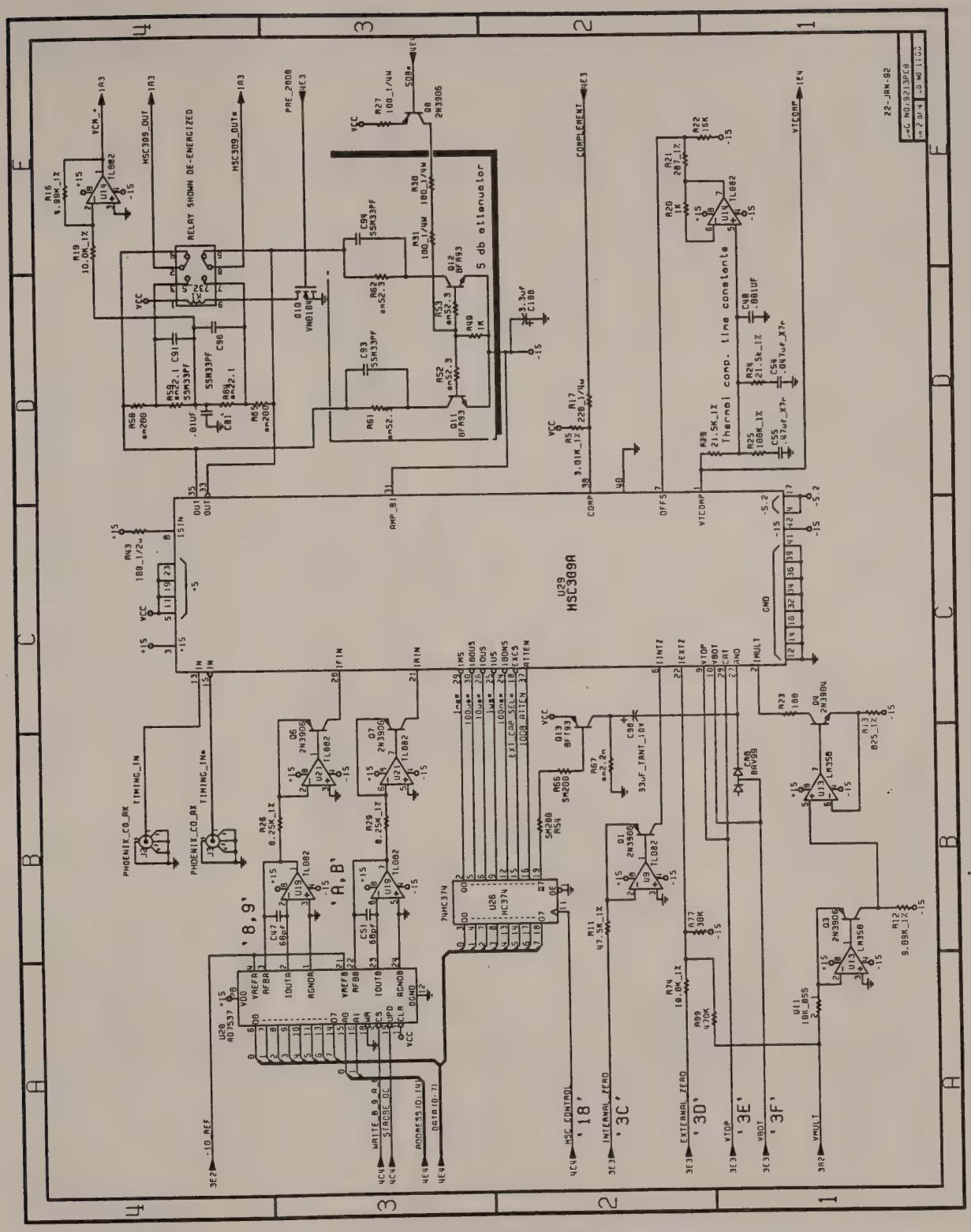
92 12 PO


SW1
SW2
SW3
CR40
CR38
CR39
MT8
MT9
MT10
MT11
J7
J8
J6
CR36
CR37
R98
R99
R100
R101
R106
R97
R102
Q30
Q31
Q32
K1
K2
C131
C130
C132
C134
C125
C126
C127
C128
C129
C133
R90
R91
R93
R92
R88
R89
GND4
CR30
CR31
CR32
CR33
CR34
CR35
C124
CR28
R87
CR29
CR27
MT7
C116
C117
C109
C110
R79
R81
R82
MT6
R77
R78
Q28
Q29
C101
C102
CR24
CR23
R72
R73
C98
R71
U25
MT5
R76
CR22
R75
CR21
C99
R67
R68
R66
C96
C95
C90
CR20
CR19
CR17
CR18
R62
R69
R70
R63
Q24
Q27
Q25
Q26
C97
U24
C93
C91
C92
R64
R65
C94
Q23
HS1
HS2
U26
R86
R84
R85
R83
R80
CR25
CR26

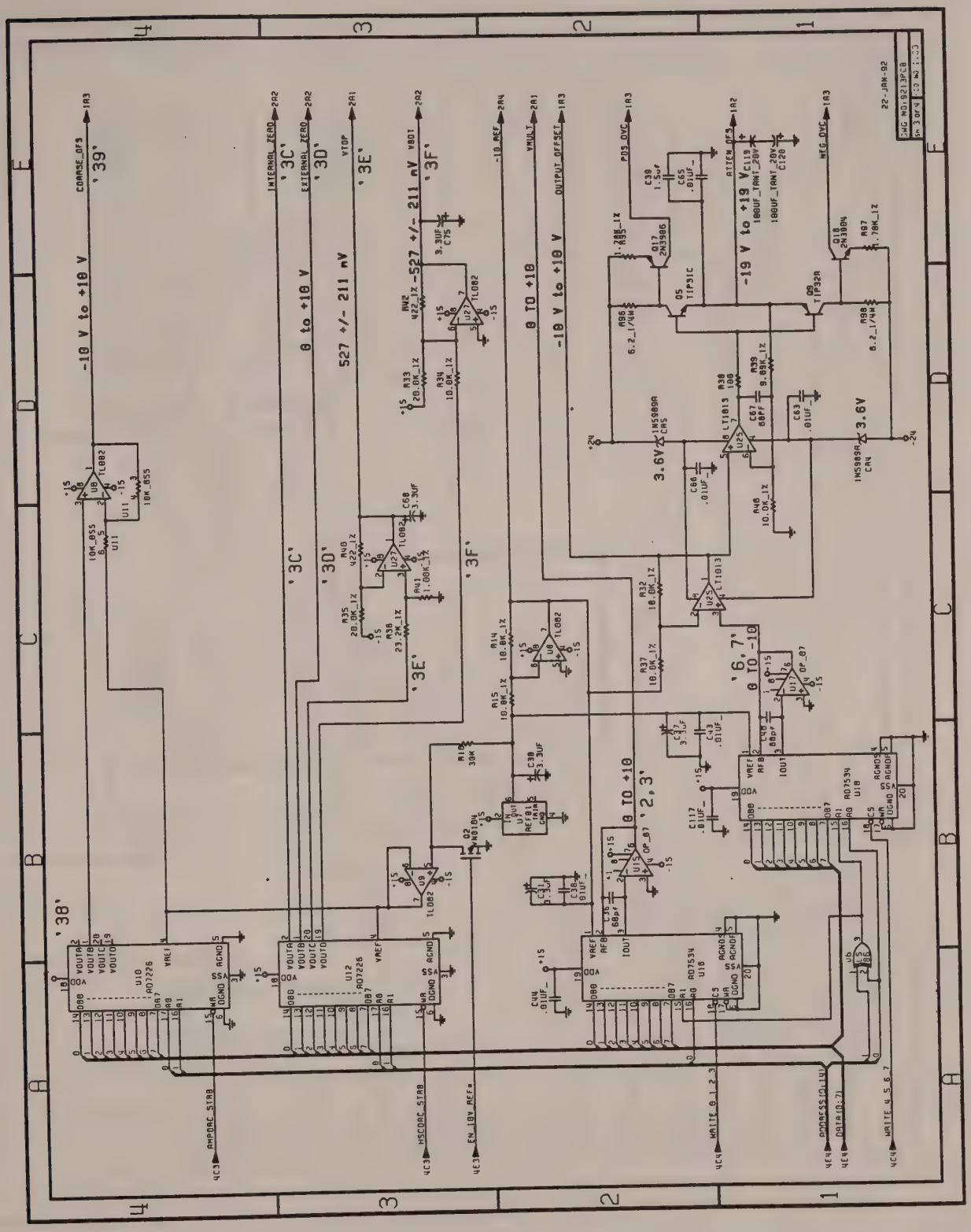
B



S12 9213 PCB Schematics Rev B-1



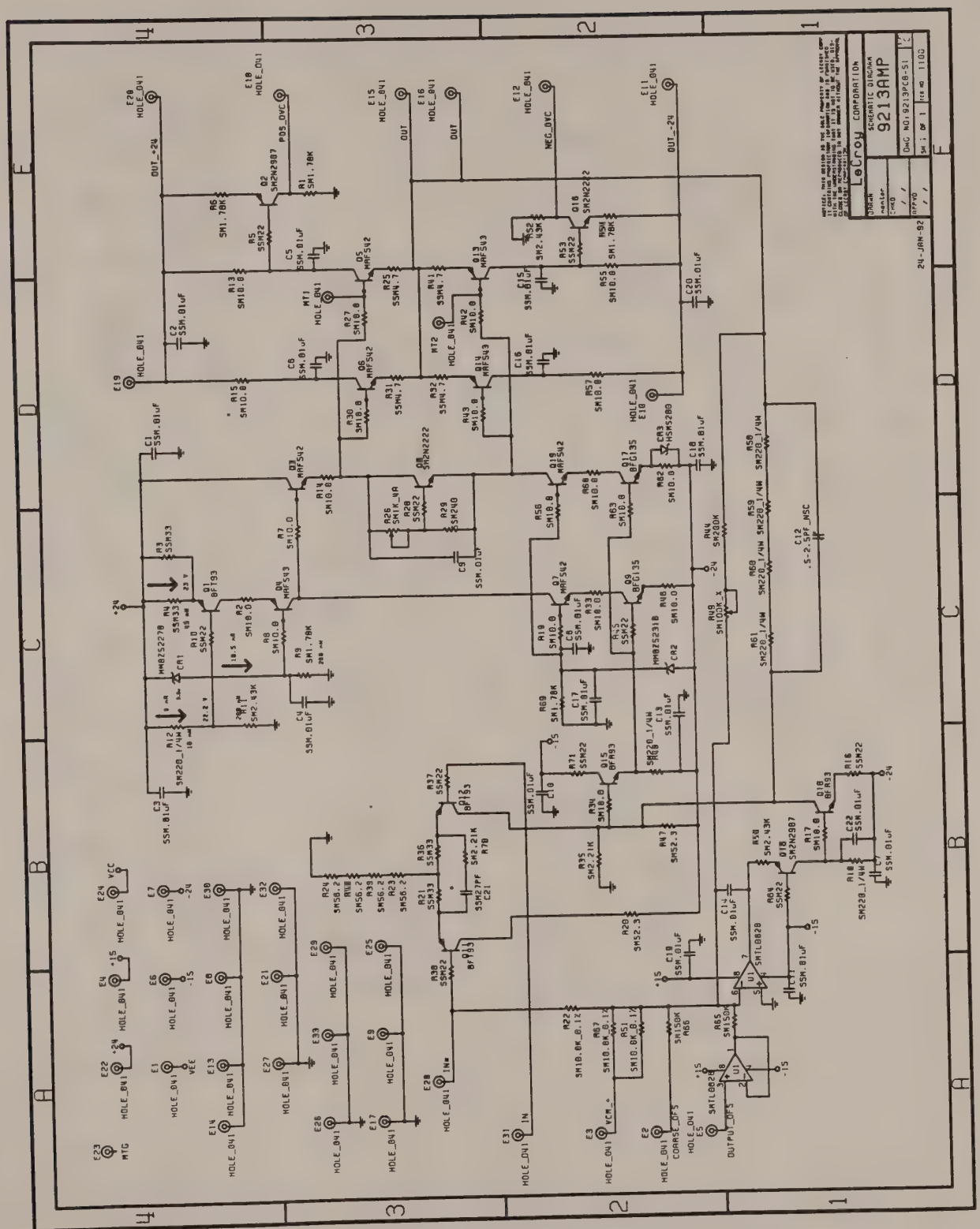
S13 9213 PCB Schematics Rev B-2



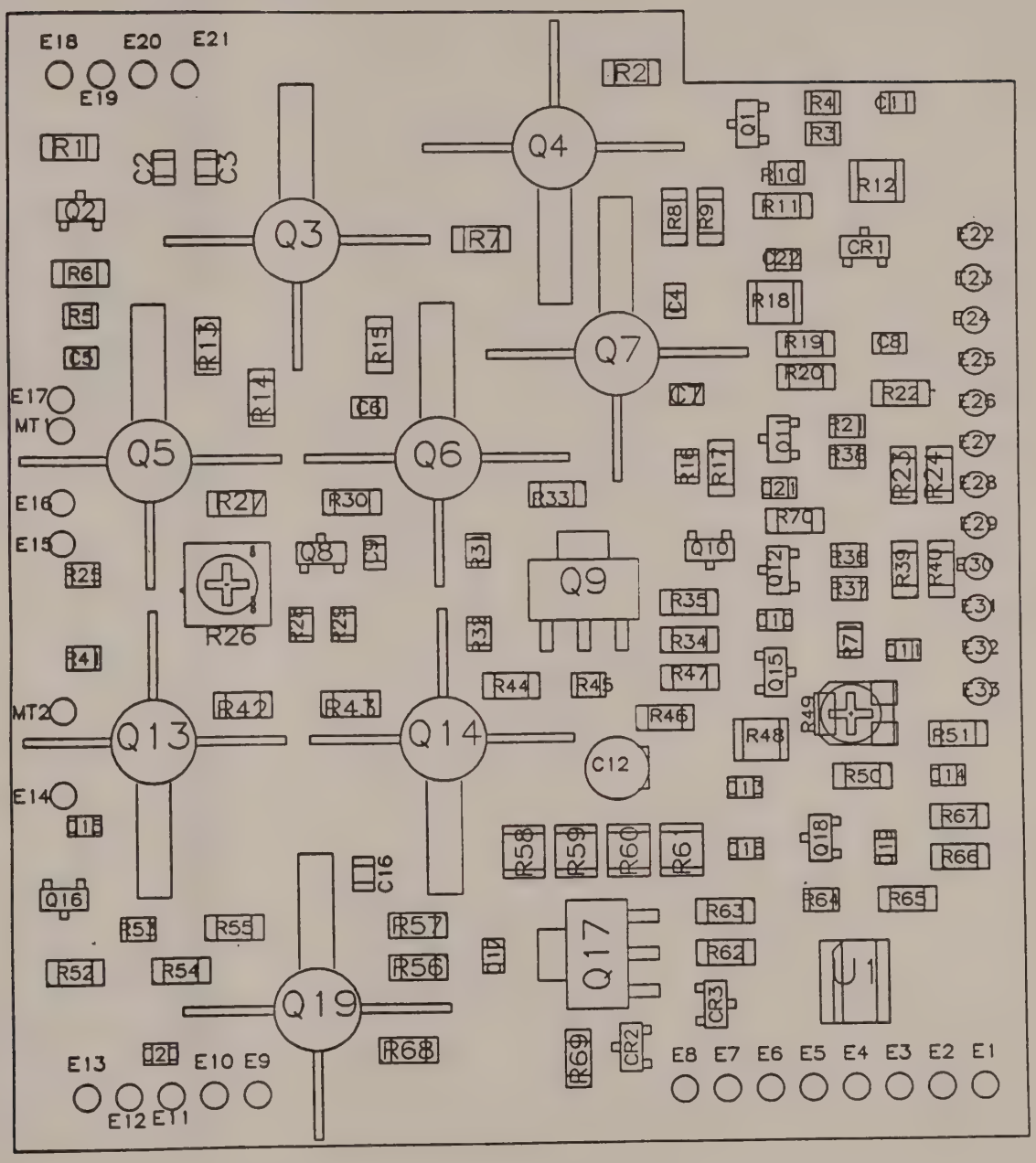
S14 9213 PCB Schematics Rev B-3

S15 9213 PCB Schematics Rev B-4

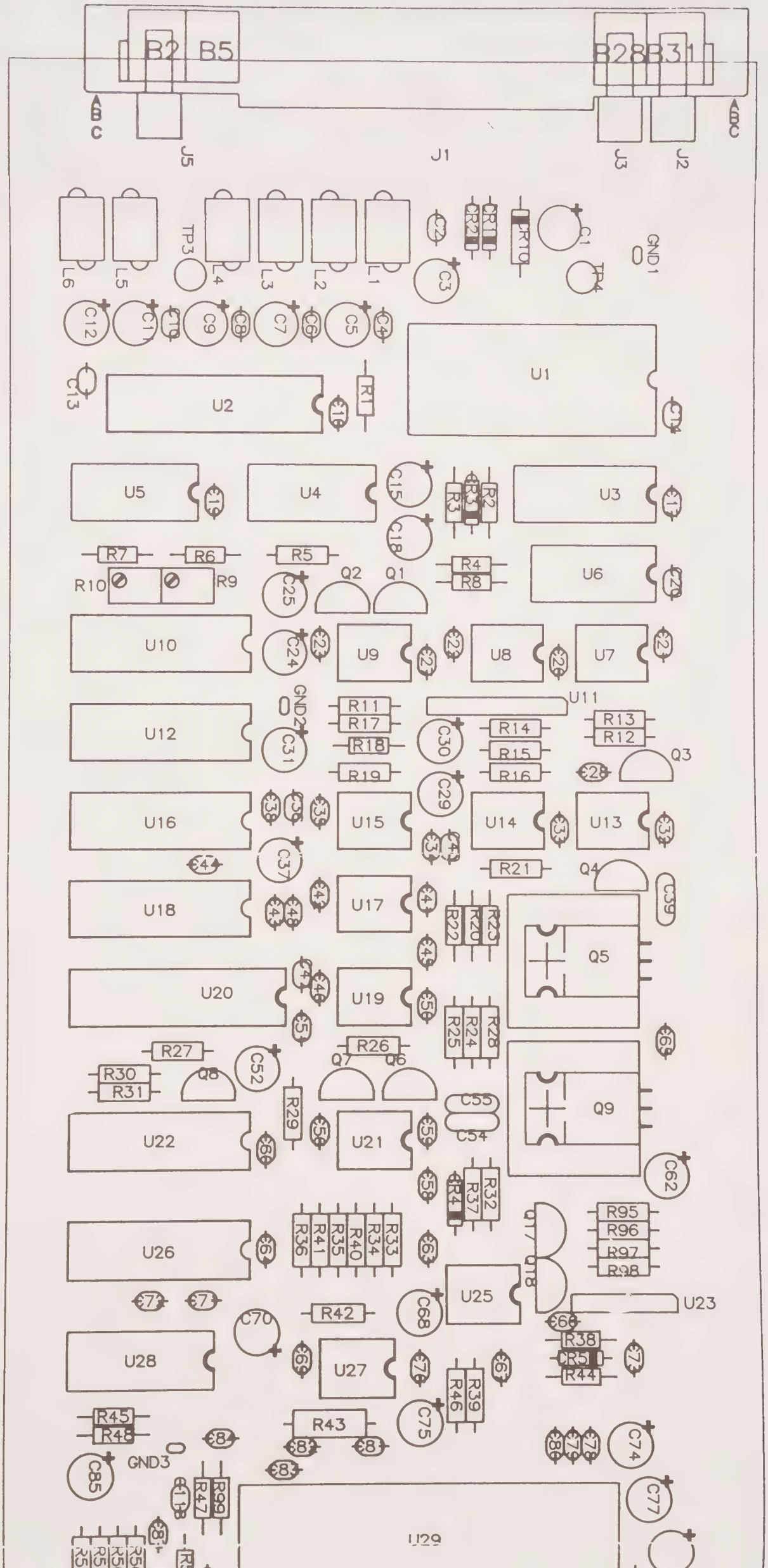
F7.1 9211/9212/9213 Module Assembly



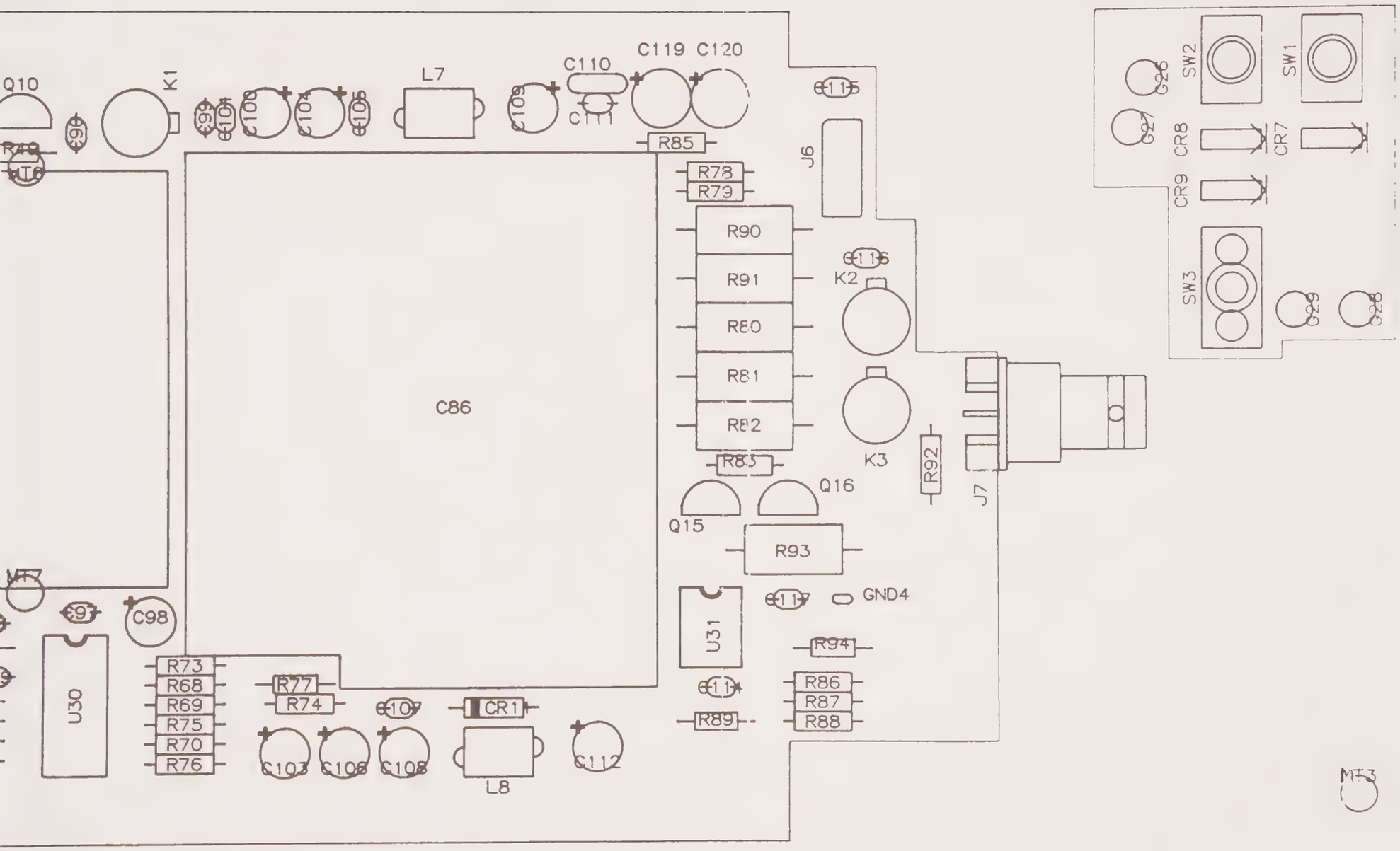
S16 9213 AMP Schematics Rev B-1

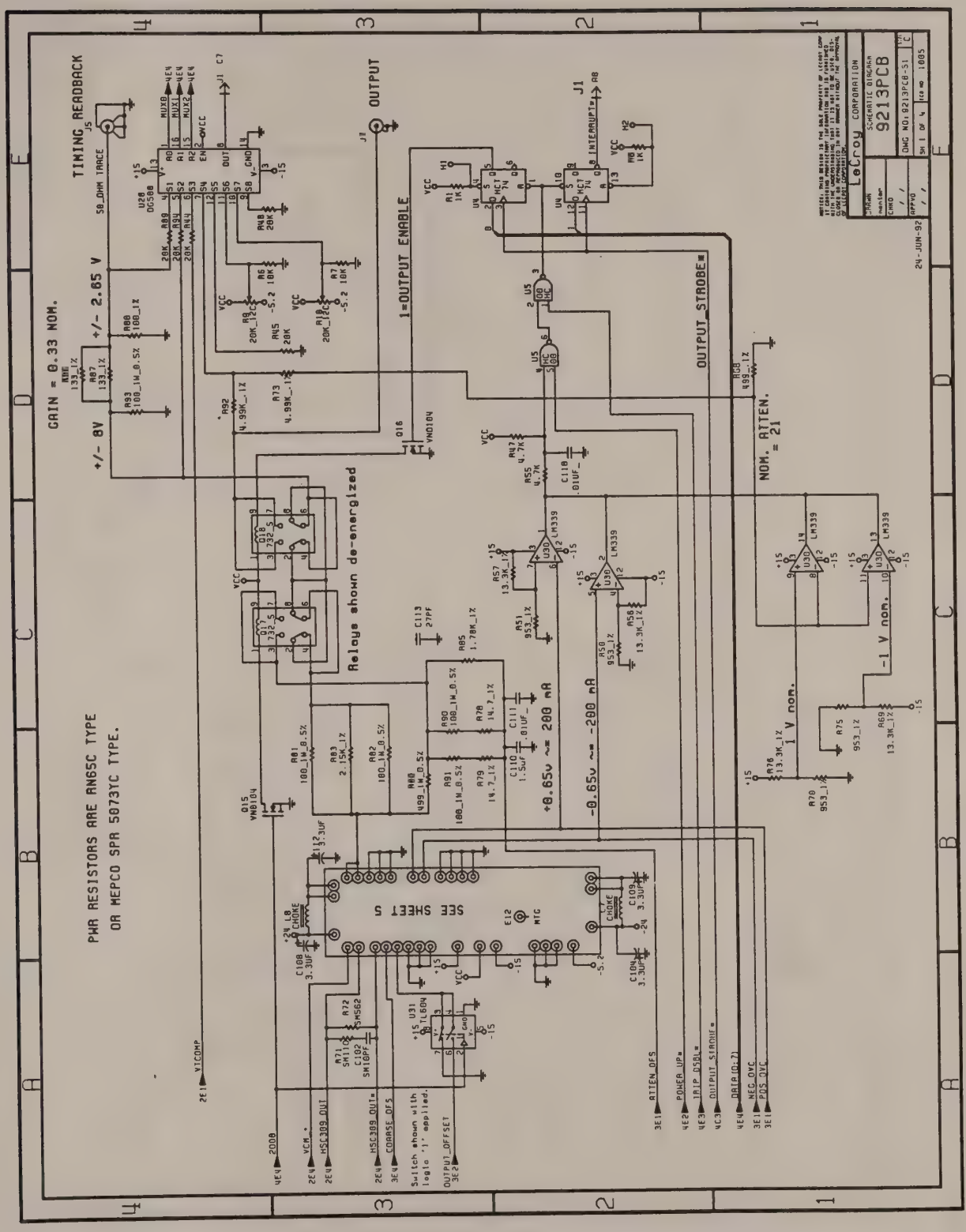

E18
E20
E21
E19
R2
R4
C1
R3
Q1
Q4
R1
C2
C3
R10
R12
Q2
Q3
R7
R8
R9
R11
CR1
R6
C22
R18
R5
C4
R13
R15
Q7
R19
C8
C5
R20
R22
E17
MT1
R14
C6
C7
Q5
Q6
R21
R38
R23
R24
R16
R17
Q11
E16
R27
R30
R33
Q21
R70
E15
Q8
Q10
Q12
R36
R39
R40
R25
Q9
R37
R35
R26
R34
R41
R47
Q15
R44
R45
MT2
R42
R43
R46
R49
Q13
Q14
R48
R51
C12
R50
E14
R67
R58
R59
R60
R61
Q18
R66
C16
Q16
R64
R65
R63
R53
R55
R57
Q17
R62
R52
R54
R56
U1
Q19
CR3
R68
R69
CR2
E13
E10
E9
E8
E7
E6
E5
E4
E3
E2
E1
E12
E11

9213 AMP

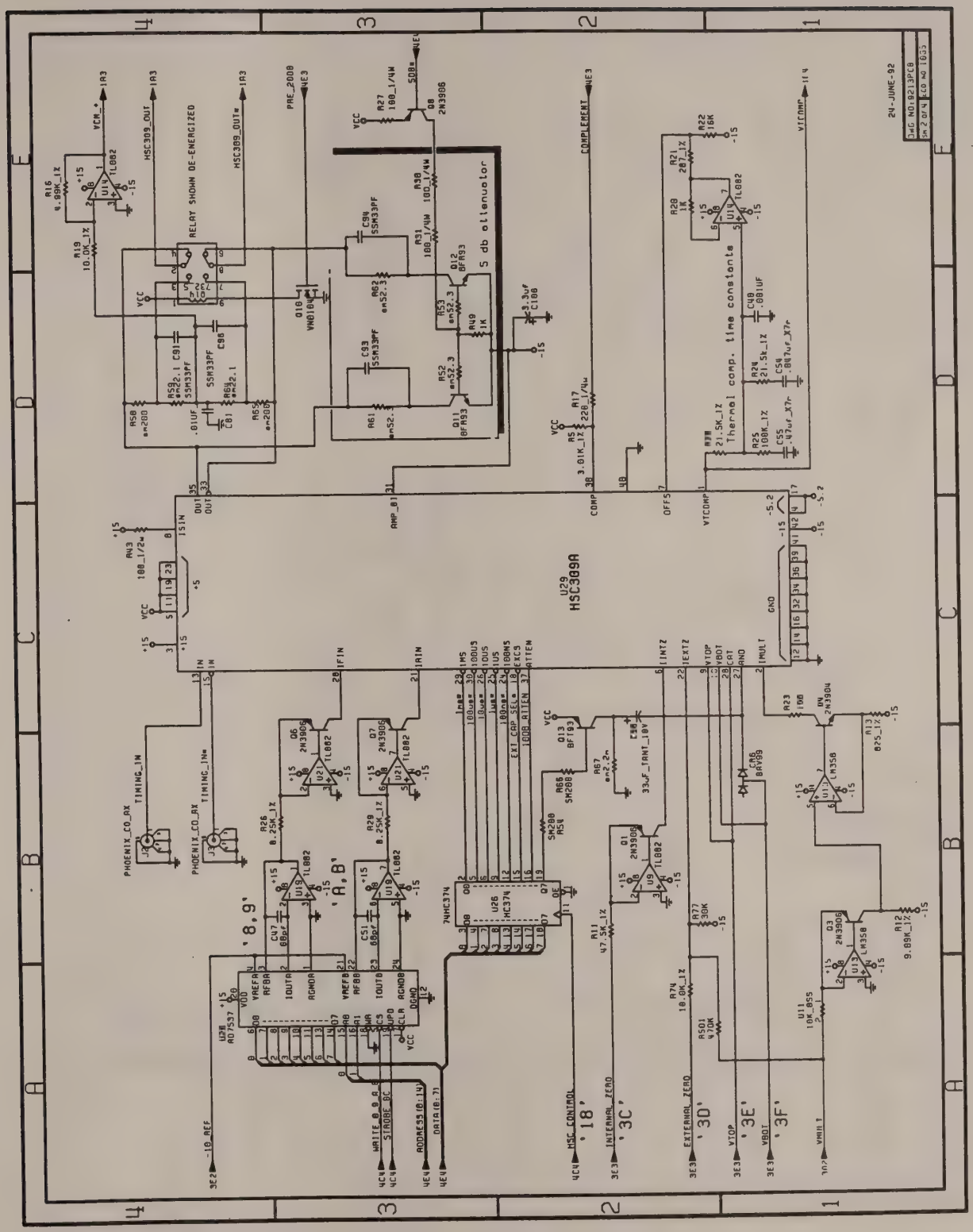

B2
B5
B28
B31
J5
J1
J3
J2
L6
L5
TP3
L4
L3
L2
L1
C2
C3
R11
R21
R10
C1
TP4
GND1
C12
C11
C10
C9
C8
C7
C6
C5
C4
C13
U2
R1
U1
U5
U4
C15
C18
R2
R3
U3
R7
R6
R5
R10
R9
Q2
Q1
C25
R4
R8
U6
U10
C24
U9
U8
U7
GND2
C31
U11
R11
R17
R18
R19
C30
R14
R15
R16
R13
R12
Q3
U12
C29
U16
U15
U14
U13
C37
R21
Q4
C39
U18
U17
R22
R20
R23
Q5
U20
U19
R25
R24
R28
R27
R30
R31
Q8
C52
R26
Q7
Q6
R29
C55
C54
U22
U21
Q9
C62
R32
R37
R34
U26
R36
R41
R35
R40
R33
Q17
Q18
R95
R96
R97
R98
U25
U23
C68
C70
R42
R38
R5
R44
U28
U27
R39
R46
C75
R45
R48
R43
C85
GND3
C74
C77
R47
R99
U29

9213PCB

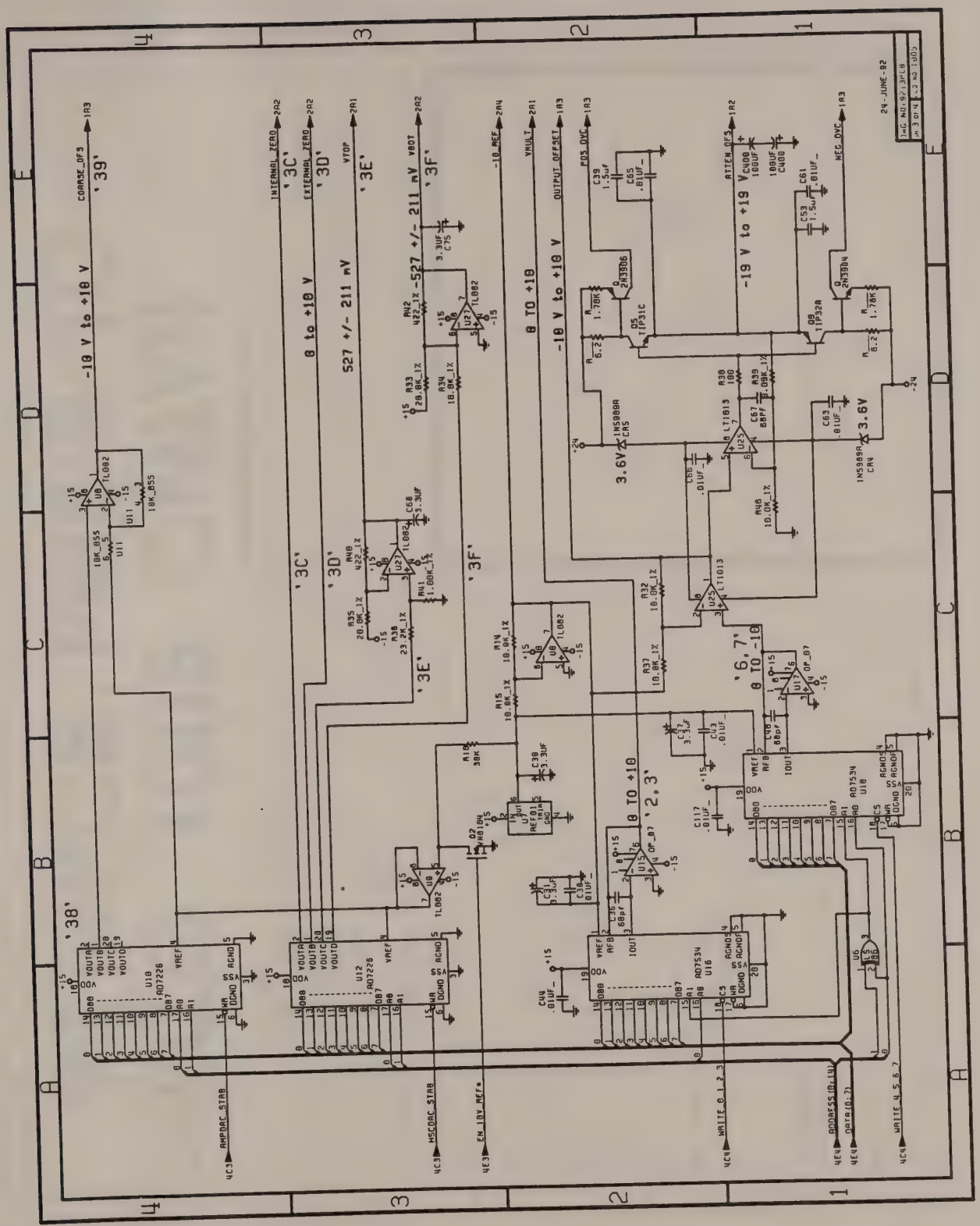

Q10
K1
L7
C110
C119
C120
C111
R85
J6
R78
R79
R90
R91
R80
R81
R82
K2
K3
C86
R83
Q16
Q15
R92
J7
R93
GND4
U31
R94
R86
R87
R88
R89
C98
U30
R73
R68
R69
R75
R70
R76
R77
R74
CR1
L8
C112
SW2
SW1
CR8
CR7
CR9
SW3
MT3



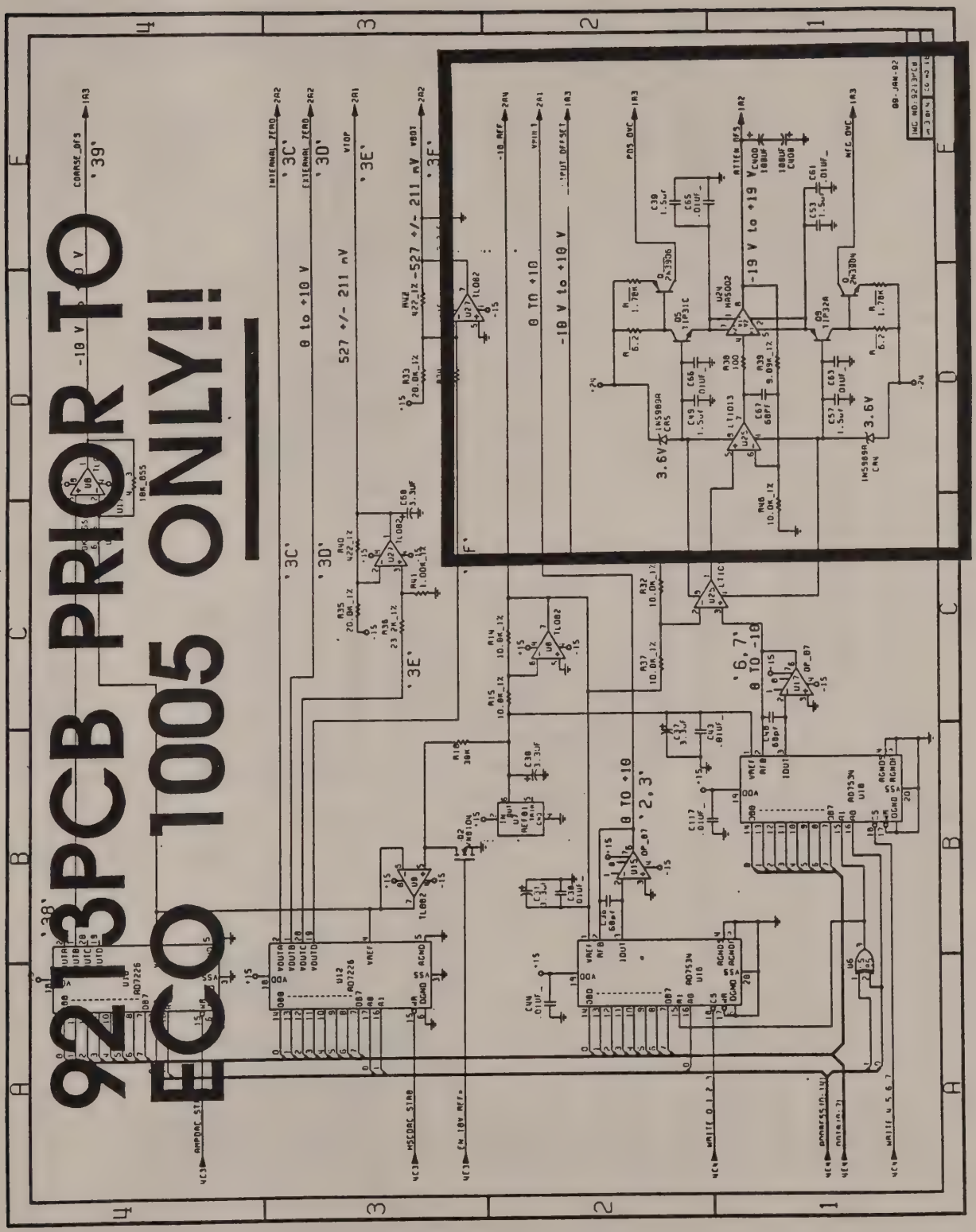
S17 9213 PCB Schematics Rev A-1



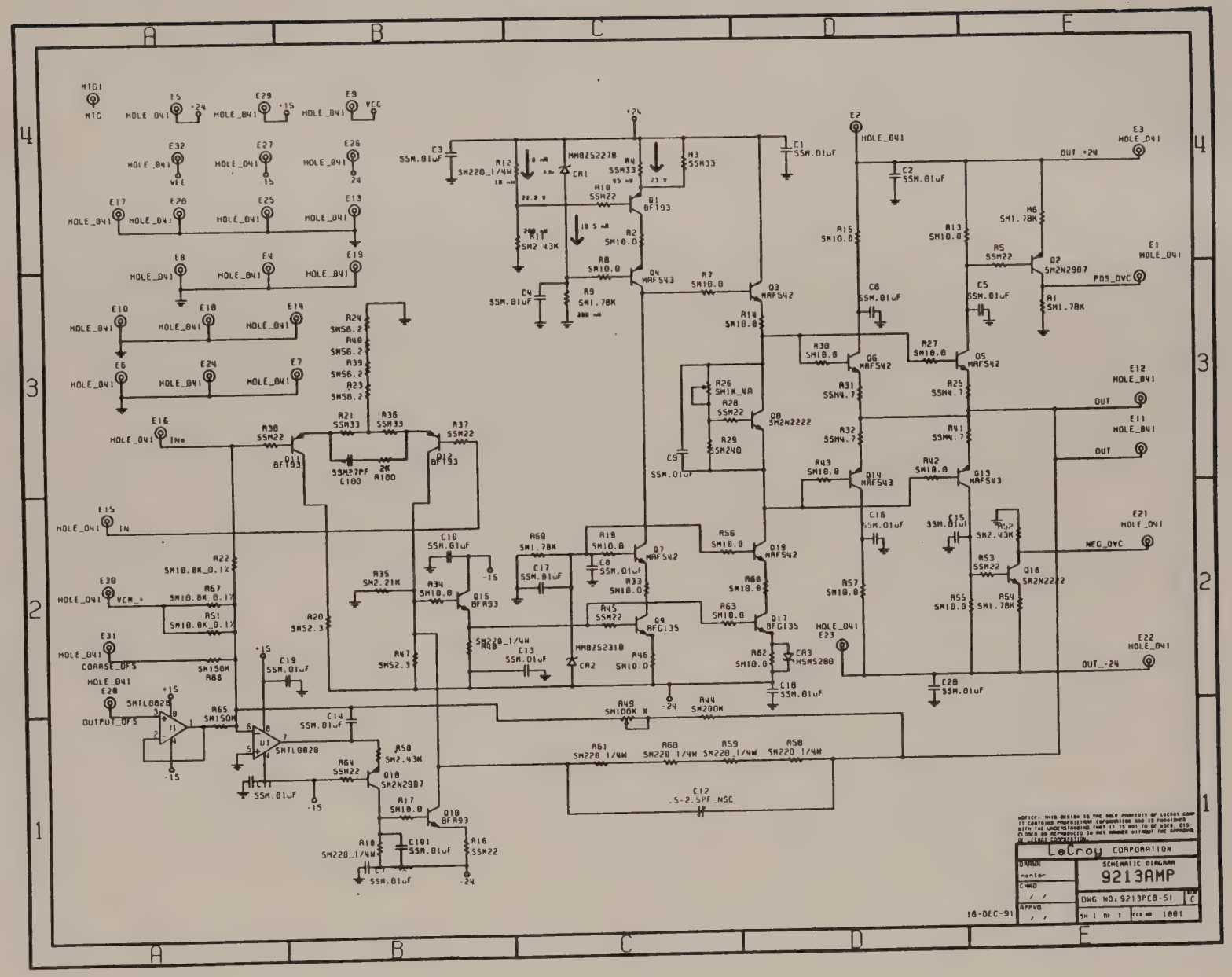
S18 9213 PCB Schematics Rev A-2



S19 9213 PCB Schematics Rev A-3



S19A 9213 AMP Schematics Rev A-3 Prior to ECO 1005 ONLY



S21 9213 AMP Schematics Rev A-1

8.0 9211 Parts List

COMPONENT #	DESCRIPTION REMARKS	QTY
1000		
428100016	KEYPAD 3-KEY ELASTOMERIC	1
555511005	SCREW SELF-TAPPING PHIL HD	2
555921041	SHOULDER SCREW 4-40	2
567632005	SCREW FLAT PHIL 6-32X5/16	2
709210026	PLUG-IN BEZEL	1
709210028	PLUG-IN GUIDE RAILS, TOP	1
709210044	PLUG-IN GUIDE RAIL, BOTTOM	1
709211036	PLUG-IN OVERLAY TRIM 9211	1
739210029	PLUG-IN SIDE PANELS	2
9211PCB	COMPLETED BOARD 9211	1

8.1 9211 PCB Parts List

COMPONENT #	DESCRIPTION REMARKS	QTY
1007		
102412100	CAP CERA DISC 100V 10 PF	1
102412560	CAP CERA DISC 100V 56 PF	2
102412680	CAP CERA DISC 100V 68 PF C37,C44,C45,C50,C61	5
103326473	CAP CERA MONO 50V .047UF C57,C95	2
103336474	CAP CERA MONO 50V .47 UF C54	1
103347155	CAP CERA MONO 50V 1.5 UF C77,C89,C92,C108 C110,C112	6
106425102	CAP CERA MONO .001UF C38	1
106425103	CAP CERA MONO .01UF C2,C4,C6,C8,C10,C12, C14,C16,C17,C20-C23, C25,C26,C29,C30,C33- C36,C39-C43,C46,C47, C51,C53,C55,C56,C58, C60,C62,C64,C65,C67, C69,C72,C74-C76,C78, C79,C90,C94,C97-C101 C103-C107,C109, C111,C113-C118	65
141268476	CAP TANT DIP CASE 10V 47UF	1
141838335	CAP TANT DIP REEL 3.3UF C1,C3,C5,C7,C9,C11, C13,C15,C18,C19,C24, C27,C28,C31,C32,C48, C49,C52,C59,C63, C68,C70,C71,C73,C80- C82,C91,C93,C102	30
142824685	CAP TANT DIP CASE 6.8 UF	1
161030000	RES COMP ZERO OHMS R46	1
161225101	RES CARBON FILM 100 OHMS R15,R33,R34,R45	4
161225102	RES CARBON FILM 1 K R4,R5,R14,R41,R58, R70	7
161225163	RES CARBON FILM 16 K	1
161225203	RES CARBON FILM 20 K R37,R73,R95-R97,R100 R101	7
161225303	RES CARBON FILM 30 K R6,R62,R64	3
161225304	RES CARBON FILM 300 K R3	1
161225363	RES CARBON FILM 36 K R59	1
161225431	RES CARBON FILM 430 OHMS	2
161225470	RES CARBON FILM 47 OHMS R18	1
161225472	RES CARBON FILM 4.7 K R71,R74,R83,R86	4
161225511	RES CARBON FILM 510 OHMS R44	1
161225514	RES CARBON FILM 510 K	1
161225753	RES CARBON FILM 75 K	1

9211 PCB Parts List

COMPONENT #	DESCRIPTION REMARKS	QTY
1007		
	R63	
161335101	RES CARBON FILM 100 OHMS R38,R39	2
161335200	RES CARBON FILM 20 OHMS R35,R36	2
161335221	RES CARBON FILM 220 OHMS R2	1
161445101	RES CARBON FILM 100 OHMS R40	1
168139285	RES RN55E .1% 75.0 OHMS R91-R94,R98,R99	6
168139326	RES RN55E .1% 200 OHMS R87-R90	4
168531341	RES PREC RN55D 287 OHMS R21	1
168531357	RES PREC RN55D 422 OHMS R30,R31 110 R29	2
168531365	RES PREC RN55D 511 OHMS R29	1
168531385	RES PREC RN55D 825 OHMS R12	1
168531401	RES PREC RN55D 1.21 K R76,R79	2
168531410	RES PREC RN55D 1.50 K R9	1
168531431	RES PREC RN55D 2.49 K R22,R78,R85	3
168531439	RES PREC RN55D 3.01 K R1	1
168531460	RES PREC RN55D 4.99 K R56,R60,R67	3
168531469	RES PREC RN55D 6.19 K R7	1
168531481	RES PREC RN55D 8.25 K R51	1
168531485	RES PREC RN55D 9.09 K R10,R24,R25	3
168531489	RES PREC RN55D 10.0 K R17,R23,R57,R61,R66, R75,R81,R82	8
168531518	RES PREC RN55D 20.0 K R26-R28	3
168531521	RES PREC RN55D 21.5 K R13,R19,R69	3
168531533	RES PREC RN55D 28.7 K R32	1
168531541	RES PREC RN55D 34.8 K R77,R84	2
168531547	RES PREC RN55D 40.2 K R80	1
168531554	RES PREC RN55D 47.5 K R8	1
168531585	RES PREC RN55D 100 K R20,R65,R68	3
190662101	RESISTOR NETWORK 100 OHMS U25	1
190832103	RESISTOR NETWORK 10 K	4

9211 PCB Parts List

COMPONENT #	DESCRIPTION REMARKS	QTY
1007		
	U11,U12,U24,U26	
200331074	IC D-TYP FLOP 74HCT74 U3,U4	2
200332000	IC 2-INPUT NAND MM74HC00 U5	1
200370374	IC OCTAL FLOP 74HC374 U23,U27	2
200380154	IC 4-TO-16 DECODR 74HC154 U2	1
205370256	IC UV E-PROM 27256G-25 U1 GIVE TO SSD MANUF.	1
207270226	IC QUAD 8-BIT CMOS DAC AD7226 U9,U10	2
207287537	IC 12-BIT DAC 7537 U17,U20	2
207340508	IC 8-CH ANALOG MPLX DG508 U30	1
208011007	IC DUAL OP AMP LM358N U15,U37	2
208011010	IC PMOS ANALOG SW TL604CP U35	1
208011011	IC JFET OP AMP TL082CP U6,U7,U13,U16,U18, U21,U22,U28,U32	9
208031010	IC QUAD DIFF COMP LM339N U36	1
208110007	IC LO OFFSET OP AMP OP-07 U19,U34	2
208111013	IC DUAL PREC OP AMP LT1013 U29	1
208950001	IC VOLT REF (+10V) REF-01 U14	1
229020089X	TRANS VOLT SUPPR P6KE11 CR11,CR12	2
230110005	DIODE SWITCHING 1N4448 CR1-CR6	6
256200001	DIODE LED RECTANGULAR RED CR14	1
256400001	DIODE LED RECTANGULAR YEL CR13	1
256500001	DIODE LED RECTANGULAR GRN CR15	1
270170904X	TRANSISTOR NPN 2N3904 Q4,Q15	2
271130002	TRANSISTOR NPN PWR TIP31C Q11,Q14,Q16	3
275170906X	TRANSISTOR PNP 2N3906 Q2,Q5-Q10	7
280170104X	TRANSISTOR FET N VN104N3 Q1,Q17,Q18,Q21	4
280190531	TRANSISTOR FET "N" IRF531 Q3	1
300050001	CHOKE FERRITE SINGLE LEAD L3-L8	6
400062228	SOCKET IC AUTO INSERTION DIP 28	1
402100000	CONN CO-AX PC MTG	3
402110302	CONN CO-AX PC MTG BNC J8,J9	2

9211 PCB Parts List

COMPONENT #	DESCRIPTION REMARKS	QTY
1007		
	GIVE TO SSD MANUF.	
403119010	HDR DBL ROW RT ANGL 10 J7	1
405764112	SOCKET SINGLE WIRE 12-POS	2
405764121	SOCKET SINGLE WIRE 21-POS	2
430540732	RELAY 2 FORM C 5V DPDT Q19,Q20,Q22	3
454121010	HDR SOLD TAIL/FEM 10 P1	1
454611064	CONN SOLD TAIL/MALE 64 J2	1
500120003	MOUNTING PAD 10-LEAD RED	3
500860302	INSULATOR FOR TO-220	1
505070002	HEAT SINK FOR TO-220	2
507052101	HEAT SINK 9211 GIVE TO SSD MANUF.	1
510160001	GROUND LUG SPADE TYPE *** *** GND1-GND4	4
521440008	SPACER HEX 4-40X1/4	2
555462002	NUT SELF-CLINCHING 4-40	2
560440004	SCREW PHILIPS 4-40X1/4	4
560440004		5
574409005	WASHER SHOULDER NYLON #4	1
576410001	WASHER SPLIT LOCK SIZE 4	4
576410001		6
719211001	PC BD PREASS'Y 9211PCB	1
HAT310	HYBRID ATTENUATOR HAT310 U38	1
HSC309	IC SLOPE CONDITIONER HSC309 GIVE TO SSD MANU. U31	1
HVV304	IC VOLTAGE AMPLIFIER GIVE TO SSD MANU. U33	1
SM236030099	DIODE SO-PKG BAV99 CR7-CR10	4
SM270030093	TRANSISTOR NPN BFR93 Q12-Q13	2
SM652101111	RES CHIP (E24) 1% 110 OHMS R53,R54	2
SM652101560	RES CHIP (E96) 56.2 OHMS R52,R55	2
SM653181266	RES THICK FILM 1% 47.5 OHMS R42,R43,R47-R50	6
SM661255056	CAP CERA CHIP 5.6 PF C83-C86	4
SM661255330	CAP CERA CHIP 5% 33 PF C87-C88	2

8.2 9212 Parts List

	COMPONENT #	DESCRIPTION REMARKS	QTY
1000			
	402900001	DUST CAP RED VINYL FOR SMA	2
	428100016	KEYPAD 3-KEY ELASTOMERIC	1
	555511005	SCREW SELF-TAPPING PHIL HD	2
	555921041	SHOULDER SCREW 4-40	2
	567632005	SCREW FLAT PHIL 6-32X5/16	2
	709210028	PLUG-IN GUIDE RAILS, TOP	1
	709210044	PLUG-IN GUIDE RAIL, BOTTOM	1
	709212026	PLIG-IN BEZEL 9212	1
	709212036	PLUG-IN OVERLAY TRIM 9212	1
	739210029	PLUG-IN SIDE PANELS	2
	9212PCB	COMPLETED BOARD 9212	1

8.3 9212 PCB Parts List

	COMPONENT #	DESCRIPTION REMARKS	QTY
1206			
	102484471	CAP CERA DISC 100V 470 PF C124	1
	103347155	CAP CERA MONO 50V 1.5 UF C66,C87,C89,C91,C116 C125,C127,C129	8
	106425102	CAP CERA MONO .001UF C31,C117,C128,C133	4
	106425103	CAP CERA MONO .01UF C2,C4,C6,C8,C10,C13 C14,C18,C19,C22,C24 C25,C26,C27,C29,C30 C33,C34,C35,C36,C37 C38,C40,C41,C42,C43 C44,C45,C46,C48,C49 C50,C53,C54,C55,C58 C60.C61,C62,C67,C69 C70,C71,C73,C75,C77 C79,C80,C84,C88,C92 C93,C95,C97 C103,C104,C105,C106 C107,C108,C111,C112 C113,C114,C115,C118 C119,C120,C121,C122 C123,C126,C130,C132 C134	75
	106443221	CAP CERA MONO 220PF C32	1
	141838335	CAP TANT DIP REEL 3.3UF C1,C3,C5,C7,C9,C11 C12,C15,C16,C17,C20 C21,C23,C28,C39,C47 C51,C52,C56,C57,C59 C63,C64,C65,C68,C72 C74,C76,C78,C81,C82 C83,C85,C86,C90,C94 C98,C99,C101,C102 C109,C131	42
	142124476	CAP TANT DIP CASE 47 UF C110	1
	161225101	RES CARBON FILM 100 OHMS R3,R7,R19,R21,R24 R36,R46 R99,R100	13
	161225102	RES CARBON FILM 1 K R20,R30,R44,R66,R87	5
	161225103	RES CARBON FILM 10 K R26,R48,R55,R56	4
	161225132	RES CARBON FILM 1.3 K R13,R28	2
	161225152	RES CARBON FILM 1.5 K R34	1
	161225162	RES CARBON FILM 1.6 K R18,R81,R82	3
	161225182	RES CARBON FILM 1.8 K R107,R59	2
	161225203	RES CARBON FILM 20 K R22,R37,R86,R97	4
	161225301	RES CARBON FILM 300 OHMS, R85,R106	2

9212 PCB Parts List

COMPONENT #	DESCRIPTION REMARKS	QTY
1206		
161225331	RES CARBON FILM 330 OHMS R9,R23	2
161225334	RES CARBON FILM 330 K 1 R27	
161225391	RES CARBON FILM 390 OHMS R51	1
161225472	RES CARBON FILM 4.7 K 6 R10,R43,R67,R68,R80 R83	
161225473	RES CARBON FILM 47 K 2 R2 R52	
161225510	RES CARBON FILM 51 OHMS R45,R49,R50	3
161225513	RES CARBON FILM 51 K 1 R32	
161335047	RES CARBON FILM 4.7 OHMS R75,R76	2
161335511	RES CARBON FILM 510 OHMS	2
161445056	RES CARBON FILM 5.6 OHMS R1	1
168531257	RES PREC RN55D 38.3 OHMS R64	1
168531277	RES PREC RN55D 61.9 OHMS R64,R65	2
168531313	RES PREC RN55D 147 OHMS R77	1
168531326	RES PREC RN55D 200 OHMS R88,R89,R92,R93	4
168531350	RES PREC RN55D 357 OHMS R29	1
168531351	RES PREC RN55D 365 OHMS R60	1
168531357	RES PREC RN55D 422 OHMS R73	1
168531362	RES PREC RN55D 475 OHMS R78	1
168531365	RES PREC RN55D 511 OHMS R12,R16,R17	3
168531372	RES PREC RN55D 604 OHMS R57	1
168531391	RES PREC RN55D 953 OHMS R6,R39	2
168531393	RES PREC RN55D 1.00 K R61	1
168531402	RES PREC RN55D 1.24 K R72	1
168531405	RES PREC RN55D 1.33 K R25	1
168531406	RES PREC RN55D 1.37 K R58	1
168531457	RES PREC RN55D 4.64 K R15	1
168531460	RES PREC RN55D 4.99 K R35,R47	2
168531485	RES PREC RN55D 9.09 K R8	1
168531489	RES PREC RN55D 10.0 K R33,R40,R79	3

9212 PCB Parts List

	COMPONENT #	DESCRIPTION REMARKS	QTY
1206			
	168531495	RES PREC RN55D 11.5 K R31	1
	168531501	RES PREC RN55D 13.3 K R4	1
	168531505	RES PREC RN55D 14.7 K R5	1
	168531518	RES PREC RN55D 20.0 K R14,R38,R41	3
	168531529	RES PREC RN55D 26.1 K R84	1
	168531532	RES PREC RN55D 28.0 K R11	1
	180247203	RES VARI CERMET 20 K R53,R54	2
	180247500	RES VARI CERMET 50 OHMS R42,R500	2
	190662101	RESISTOR NETWORK 100 OHMS U21	1
	200332000	IC 2-INPUT NAND MM74HC00 U3	1
	200342138	IC 3-TO-8 LN DEC 74HC138 U2	1
	200370374	IC OCTAL FLOP 74HC374	1
	200372273	IC D-TYP FLOP 74HC273 U18	1
	205370256	IC UV E-PROM 27256G-25 U1	1
	206143175	IC QUAD D FLIP FLOP 74HCT175 U4	1
	207270226	IC QUAD 8-BIT CMOS DAC AD7226 U10	1
	207280526	IC QUAD 12-BIT DAC 526 U14	1
	207340508	IC 8-CH ANALOG MPLX DG508 U20	1
	208011007	IC DUAL OP AMP LM358N U6,U7,U8,U13,U17	5
	208011011	IC JFET OP AMP TL082CP U9,U11,U16,U22,U24	5
	208031010	IC QUAD DIFF COMP LM339N U5	1
	208111013	IC DUAL PREC OP AMP LT1013 U12	1
	208122337	IC ADJ -VOLT REG LM337T U15	1
	208510317	IC ADJ +V REG 317LZ Q28,Q29	2
	208570317	IC ADJ +V REG LM317 U23	1
	208590337	IC VOLT REG NEG ADJ LM337 Q3,Q5,Q10,Q24,Q25	5
	208950001	IC VOLT REF (+10V) REF-01 U19	1
	229020055X	TRANS VOLT SUPPR P6KE6.8 CR13,CR16,CR25,CR26	4
	229020089X	TRANS VOLT SUPPR P6KE11 CR28,CR29	2
	229020128	TRANS VOLT SUPPR PKE15A CR14,CR15	2

9212 PCB Parts List

	COMPONENT #	DESCRIPTION REMARKS	QTY
1206	230110005	DIODE SWITCHING 1N4448 CR1 ------- CR9 CR11,CR12	11
	235010005	DIODE RECTIFIER 1N4005 CR17 ------- CR24	8
	240225709	DIODE ZENER 6.2V 1N5234 CR27	1
	253050817	DIODE HOT CARRIER 1N5817 CR10	1
	256052177	DIODE LED BICOLOR RED/GRN CR36,CR37	2
	256200001	DIODE LED RECTANGULAR RED CR38	1
	256400001	DIODE LED RECTANGULAR YEL CR40	1
	256500001	DIODE LED RECTANGULAR GRN CR39	1
	270110003	TRANSISTOR NPN PN2222A Q4,Q12,Q13	3
	271130002	TRANSISTOR NPN PWR TIP31C Q19,Q21,Q22,Q23	4
	275110001	TRANSISTOR PNP P2N2907 11 Q1,Q2,Q6,Q7,Q11,Q14 Q15,Q20,Q26,Q27,Q30	
	280170104	TRANSISTOR FET N VN0104N3 Q18,Q31,Q32	3
	280190531	TRANSISTOR FET "N" IRF531 Q16	1
	281170104	TRANSISTOR FET P VP0104N3 Q17	1
	300050001	CHOKE FERRITE SINGLE LEAD L1 --------- L6	6
	400062228	SOCKET IC AUTO INSERTION DIP 28	1
	402100000	CONN CO-AX PC MTG J2,J3,J5	3
	402110006	CONN SMA FEMALE CARD EDGE J7,J8	2
	403119010	HDR DBL ROW RT ANGL 10 J6	1
	405764112	SOCKET SINGLE WIRE 12-POS	4
	430540732	RELAY 2 FORM C 5V DPDT K1,K2	2
	454121010	HDR SOLD TAIL/FEM 10 P1	1
	454611064	CONN SOLD TAIL/MALE 64 J1	1
	500120003	MOUNTING PAD 10-LEAD RED	2
	500860302	INSULATOR FOR TO-220	7
	505070002	HEAT SINK FOR TO-220	7
	507052102	HEAT SINK 9212	1
	510160001	GROUND LUG SPADE TYPE GND1,GND2 GND3,GND4	4
	519220909	LED MOUNT FOR T-1 3/4 90 DEG	2
	520000106	SPACER NYLON .200 X .250	2
	521440011	SPACER HEX 4-40X11/32	3
	555462002	NUT SELF-CLINCHING 4-40	7
	560440004	SCREW PHILIPS 4-40X1/4	3
	560440005	SCREW PHILIPS 4-40X5/16	8

9212 PCB Parts List

	COMPONENT #	DESCRIPTION REMARKS	QTY
1206			
	560440005		6
	574409005	WASHER SHOULDER NYLON #4	7
	576410001	WASHER SPLIT LOCK SIZE 4	10
	576410001		6
	719212001	PC BD PREASS'Y 9212PCB	1
	9212PS	PULSE SHRINK CIRCUIT U25	1
	SM236030099	DIODE SO-PKG BAV99 CR30 ------- CR35	6
	SM651181750	RES CHIP THIN FILM .1% 75.0 OHM R94,R95,R96,R103 R104,R105	6
	SM652101203	RES CHIP (E24) 1% 20 K R90,R91 R102	3

8.4 9213 Parts List

	COMPONENT #	DESCRIPTION REMARKS	
1000	428100016	KEYPAD 3-KEY ELASTOMERIC	1
	555511005	SCREW SELF-TAPPING PHIL HD	2
	555921041	SHOULDER SCREW 4-40	2
	567632005	SCREW FLAT PHIL 6-32X5/16	2
	709210028	PLUG-IN GUIDE RAILS, TOP	1
	709210044	PLUG-IN GUIDE RAIL, BOTTOM	1
	709213026	PLUG-IN BEZEL 9213	1
	709213036	PLUG-IN OVERLAY TRIM 9213	1
	739210029	PLUG-IN SIDE PANELS	2
	9213PCB	COMPLETED BOARD 9213	1

8.5 9213 PCB Parts List

	COMPONENT #	DESCRIPTION REMARKS	
1100			
	103100473	CAP CERA MONO .047 UF C54	1
	103336474	CAP CERA MONO 50V .47 UF C55	1
	103347155	CAP CERA MONO 50V 1.5 UF C39,C110	2
	106425102	CAP CERA MONO .001UF C40	1
	106425103	CAP CERA MONO .01UF C2,C4,C6,C8,C10,C13 C14,C16,C17,C19,C20 C21,C22,C23,C26,C27 C28,C32,C33,C34,C35 C38,C41---C46,C50 C56,C58---C61,C63 C64,C65,C66,C69,C71 C72,C73,C76,C78,C79 C80---C84,C87---C90 C97,C99,C101,C105 C107,C111,C114,C115 C116,C117,C118	64
	106443680X	CAP CERA MONO 68PF C36,C47,C48,C51,C67	5
	141838335	CAP TANT DIP REEL 3.3UF C1,C3,C5,C7,C9,C11 C12,C15,C18,C24,C25 C29,C30,C31,C37,C52 C62,C68,C70,C74,C75 C77,C85,C86,C100 C103,C104,C106,C108 C109,C112	31
	142273330	CAP TANT DIP 33UF C98	1
	142564107	CAP TANT DIP CASE 100UF C119,C120	2
	161030000	RES COMP ZERO OHMS R4	1
	161225101	RES CARBON FILM 100 OHMS R23,R38	2
	161225102	RES CARBON FILM 1 K R1,R2,R8,R20,R49	5
	161225103	RES CARBON FILM 10 K R6,R7	2
	161225163	RES CARBON FILM 16 K R22	1
	161225203	RES CARBON FILM 20 K R44,R45,R48,R89,R94	5
	161225244	RES CARBON FILM 240 K	1
	161225303	RES CARBON FILM 30 K R18,R77	2
	161225472	RES CARBON FILM 4.7 K R47,R55	2
	161225474	RES CARBON FILM 470 K R99	1
	161335062	RES CARBON FILM 6.2 OHMS R96,R98	2
	161335101	RES CARBON FILM 100 OHMS R27,R30,R31	3

9213 PCB Parts List

	COMPONENT #	DESCRIPTION REMARKS	QTY
1100			
	161335221	RES CARBON FILM 220 OHMS R17	1
	161445101	RES CARBON FILM 100 OHMS R43	1
	168139560	RES RN55E .1% 4.99 K 2 R73,R92	
	168531217	RES PREC RN55D 14.7 OHMS R78,R79	2
	168531297	RES PREC RN55D 100 OHMS 1 R88	
	168531309	RES PREC RN55D 133 OHMS 2 R86,R87	
	168531341	RES PREC RN55D 287 OHMS 1 R21	
	168531357	RES PREC RN55D 422 OHMS 2 R40,R42	
	168531385	RES PREC RN55D 825 OHMS 1 R13	
	168531391	RES PREC RN55D 953 OHMS 4 R50,R51,R70,R75	
	168531393	RES PREC RN55D 1.00 K R41	1
	168531417	RES PREC RN55D 1.78 K R85,R95,R97	3
	168531425	RES PREC RN55D 2.15 K R83	1
	168531439	RES PREC RN55D 3.01 K R5	1
	168531460	RES PREC RN55D 4.99 K R16	1
	168531481	RES PREC RN55D 8.25 K R26,R29	2
	168531485	RES PREC RN55D 9.09 K R12,R39	2
	168531489	RES PREC RN55D 10.0 K 8 R14,R15,R19,R32,R34 R37,R46,R74	
	168531501	RES PREC RN55D 13.3 K 4 R56,R57,R69,R76	
	168531518	RES PREC RN55D 20.0 K 2 R33,R35	
	168531521	RES PREC RN55D 21.5 K 2 R24,R28	
	168531524	RES PREC RN55D 23.2 K 1 R36	
	168531554	RES PREC RN55D 47.5 K 1 R11	
	168531585	RES PREC RN55D 100 K 1 R25	
	168539001	RES PREC 55D .1% 499 OHMS R68	1
	168778297	RES PREC RN65C 100 OHM 5 R81,R82,R90,R91,R93	
	168778364	RES PREC RN65C 499 OHM 1 R80	
	180247203	RES VARI CERMET 20 K 2 R9,R10	
	190662101	RESISTOR NETWORK 100 OHMS (U23)	1

9213 PCB Parts List

	COMPONENT #	DESCRIPTION REMARKS	QTY
1100			
	190832103	RESISTOR NETWORK 10 K U11	1
	200331074	IC D-TYP FLOP 74HCT74 U4	1
	200332000	IC 2-INPUT NAND MM74HC00 U5	1
	200344174	IC HEX D-FLOP 74HCT174 U3	1
	200370374	IC OCTAL FLOP 74HC374 U22,U26	2
	200380154	IC 4-TO-16 DECODR 74HC154 U2	1
	204337486	IC QUAD 2-IN XCLUS OR GATE 74HC86 U6	1
	205370256	IC UV E-PROM 27256G-25 U1	1
	207270226	IC QUAD 8-BIT CMOS DAC AD7226 U10,U12	2
	207277534	IC 14-BIT CMOS DAC AD7534 U16,U18	2
	207287537	IC 12-BIT DAC 7537 U20	1
	207340508	IC 8-CH ANALOG MPLX DG508 U28	1
	208011007	IC DUAL OP AMP LM358N U13	1
	208011010	IC PMOS ANALOG SW TL604CP U31	1
	208011011	IC JFET OP AMP TL082CP U8,U9,U14,U19,U21 U27	6
	208031010	IC QUAD DIFF COMP LM339N U30	1
	208110007	IC LO OFFSET OP AMP OP-07 U15,U17	2
	208111013	IC DUAL PREC OP AMP LT1013 U25	1
	208950001	IC VOLT REF (+10V) REF-01 U7	1
	230110005	DIODE SWITCHING 1N4448 CR1,CR2,CR3	3
	235010005	DIODE RECTIFIER 1N4005 CR10,CR11	2
	240225703	DIODE ZENER 3.6V 1N5989A CR4,CR5	2
	256200001	DIODE LED RECTANGULAR RED	1
	256400001	DIODE LED RECTANGULAR YEL	1
	256500001	DIODE LED RECTANGULAR GRN	1
	270170904	TRANSISTOR NPN 2N3904 Q4,Q18	2
	271130002	TRANSISTOR NPN PWR TIP31C Q5	1
	275130001	TRANSISTOR PNP PWR TIP32A Q9	1
	275170906	TRANSISTOR PNP 2N3906 Q1,Q3,Q6,Q7,Q8 Q17	6
	280170104	TRANSISTOR FET N VN0104N3 Q2,Q10,Q15,Q16	4

9213 PCB Parts List

	COMPONENT #	DESCRIPTION REMARKS	QTY
1100			
	300050001	CHOKE FERRITE SINGLE LEAD L1,L2,L3,L4,L5 L6,L7,L8	8
	400062228	SOCKET IC AUTO INSERTION DIP 28	1
	402100000	CONN CO-AX PC MTG J2,J3,J5	3
	402110302	CONN CO-AX PC MTG BNC J7	1
	403119010	HDR DBL ROW RT ANGL 10 J6	1
	405764121	SOCKET SINGLE WIRE 21-POS	2
	430540732	RELAY 2 FORM C 5V DPDT K1,K2,K3,K4	3
	454121010	HDR SOLD TAIL/FEM 10 P1	1
	454311032	HDR SOLD TAIL/MALE 32	1
	454611064	CONN SOLD TAIL/MALE 64 J1	1
	500120003	MOUNTING PAD 10-LEAD RED	3
	500860302	INSULATOR FOR TO-220	2
	505070002	HEAT SINK FOR TO-220	2
	510160001	GROUND LUG SPADE TYPE	4
	555462002	NUT SELF-CLINCHING 4-40	2
	560440004	SCREW PHILIPS 4-40X1/4	2
	576410001	WASHER SPLIT LOCK SIZE 4	2
	719213001	PC BD PREASS'Y 9213PCB	1
	9213AMP	OUTPUT AMPLIFIER BD 9213AMP	1
	HSC309A	IC SLOPE GENERATOR U29	1
	SM236030099	DIODE SO-PKG BAV99 CR6	1
	SM270030093	TRANSISTOR NPN BFR93 Q11,Q12	2
	SM275030093	TRANSISTOR PNP BFT93 Q13	1
	SM653181234	RES THICK FILM 1% 22.1 OHMS R59,R64	2
	SM653181270	RES THICK FILM 1% 52.3 OHMS R52,R58,R65,R66	4
	SM653181301	RES THICK FILM 1% 110 OHMS R71	1
	SM653181326	RES THICK FILM 1% 200 OHMS R54,R58,R65 R66	4
	SM653181369	RES THICK FILM 1% 562 OHMS R72	1
	SM653185225	RES THICK FILM 5% 2.2 M R67	1
	SM661186100	CAP CERA CHIP 10% 10 PF C102	1
	SM661255330	CAP CERA CHIP 5% 33 PF C91,C93,C94,C96	4

8.6 9214 Parts List

	COMPONENT #	DESCRIPTION REMARKS	QTY
1000	40290000 1	DUST CAP RED VINYL FOR SMA	2
	42810016	KEYPAD 3-KEY ELASTOMERIS	1
	555511005	SCREW SELF-TAPPING PHIL HD	2
	555921041	SHOULDER SCREW 4-40	2
	567632005	SCREW FLAT PHIL 6-32X5/16	2
	709210028	PLUG-IN GUIDE RAILS, TOP	1
	709210044	PLUG-IN GUIDE RAIL, BOTTOM	1
	709212026	PLUG-IN BEZEL 9212	1
	709214036	PLUG-IN OVERLAY TRIM 9214	1
	739210029	PLUG-IN SIDE PANELS	2
	9212PCB	COMPLETED BOARD 9212	1
	HLV308A	HYB LOGIC TO VOLT HLV308A	1

www.manualsplus.com
1033869